

# Micropower, Rail to Rail Input Current Sense Amplifier with Voltage Output

## ISL28006

The ISL28006 is a micropower, uni-directional high-side and low-side current sense amplifier featuring a proprietary rail-to-rail input current sensing amplifier. The ISL28006 is ideal for high-side current sense applications where the sense voltage is usually much higher than the amplifier supply voltage. The device can be used to sense voltages as high as 28V when operating from a supply voltage as low as 2.7V. The micropower ISL28006 consumes only 50µA of supply current when operating from a 2.7V to 28V supply.

The ISL28006 features a common-mode input voltage range from 0V to 28V. The proprietary architecture extends the input voltage sensing range down to 0V, making it an excellent choice for low-side ground sensing applications. The benefit of this architecture is that a high degree of total output accuracy is maintained over the entire 0V to 28V common mode input voltage range.

The ISL28006 is available in fixed (100V/V, 50V/V, 20V/V and Adjustable) gains in the space saving 5 Ld SOT-23 package and the 6 Ld SOT-23 package for the adjustable gain part. The parts operate over the extended temperature range from -40°C to +125°C.

## Features

- Low Power Consumption . . . . . 50µA,Typ
- Supply Range. . . . . 2.7V to 28V
- Wide Common Mode Input . . . . . 0V to 28V
- Gain Versions
  - ISL28006-100 . . . . . 100V/V
  - ISL28006-50 . . . . . 50V/V
  - ISL28006-20 . . . . . 20V/V
  - ISL28006-ADJ . . . . . ADJ (Min Gain = 20V/V)
- Operating Temperature Range . . . . -40°C to +125°C
- Packages . . . . . 5 Ld SOT-23, 6 Ld SOT-23

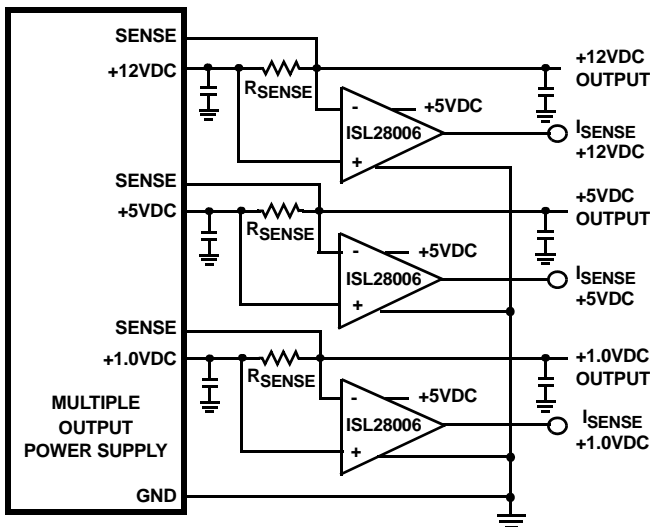
## Applications\* (see page 23)

- Power Management/Monitors
- Power Distribution and Safety
- DC/DC, AC/DC Converters
- Battery Management/Charging
- Automotive Power Distribution

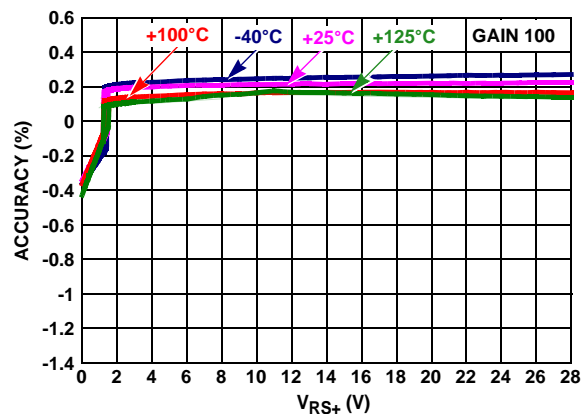
## Related Literature\* (see page 23)

- See [AN1532](#) for "ISL28006 Evaluation Board User's Guide"

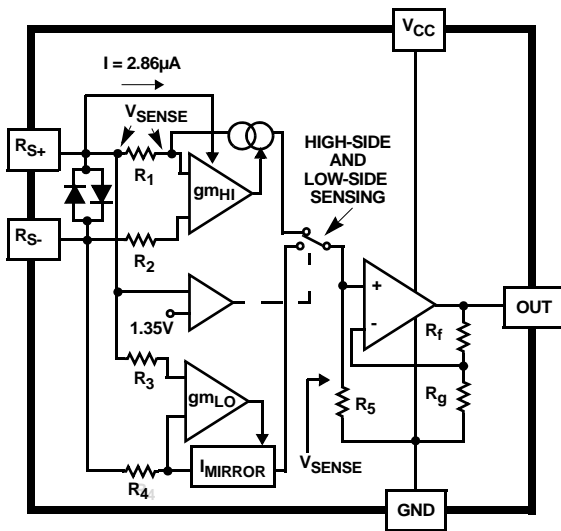
## Typical Application



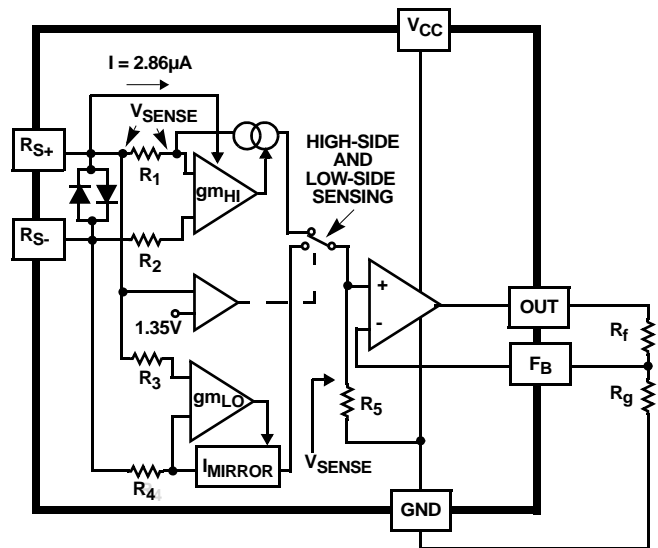
## Gain Accuracy vs $V_{RS+} = 0V$ to 28V



## Block Diagram



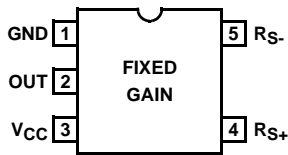
FIXED GAIN PARTS



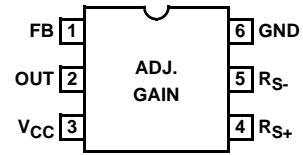
ADJUSTABLE GAIN PART

## Pin Configurations

ISL28006-100, 50, 20  
(5 LD SOT-23)  
TOP VIEW

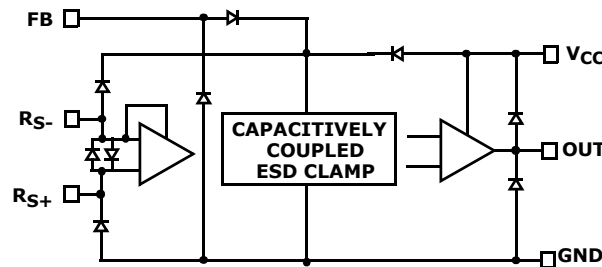


ISL28006-ADJ  
(6 LD SOT-23)  
TOP VIEW



## Pin Descriptions

ISL28006-100, 50, 20 (5 LD SOT-23)	ISL28006-ADJ (6 LD SOT-23)	PIN NAME	DESCRIPTION
1	6	GND	Power Ground
	1	FB	Input Pin for External Resistors
2	2	OUT	Amplifier Output
3	3	VCC	Positive Power Supply
4	4	RS+	Sense Voltage Non-inverting Input
5	5	RS-	Sense Voltage Inverting Input



## Ordering Information

<b>PART NUMBER (Notes 1, 2, 3)</b>	<b>GAIN</b>	<b>PART MARKING (Note 4)</b>	<b>PACKAGE Tape &amp; Reel (Pb-Free)</b>	<b>PKG. DWG. #</b>
ISL28006FH100Z-T7	100V/V	BDJA	5 Ld SOT-23	P5.064A
ISL28006FH50Z-T7	50V/V	BDHA	5 Ld SOT-23	P5.064A
ISL28006FH20Z-T7	20V/V	BDGA	5 Ld SOT-23	P5.064A
ISL28006FHADJZ-T7	ADJ	BDFA	6 Ld SOT-23	P6.064
ISL28006FH-100EVAL1Z	100V/V Evaluation Board			
ISL28006FH-50EVAL1Z	50V/V Evaluation Board			
ISL28006FH-20EVAL1Z	20V/V Evaluation Board			
ISL28006FH-ADJEVAL1Z	Adjustable Evaluation Board			

**NOTES:**

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL28006](#). For more information on MSL please see techbrief [TB363](#).
4. The part marking is located on the bottom of the part.

## Absolute Maximum Ratings

Max Supply Voltage . . . . . 28V  
 Max Differential Input Current . . . . . 20mA  
 Max Differential Input Voltage . . . . .  $\pm 0.5V$   
 Max Input Voltage ( $R_{S+}$ ,  $R_{S-}$ , FB) . . . . . GND - 0.5V to 30V  
 Max Input Current for Input Voltage <GND - 0.5V . . . . .  $\pm 20mA$   
 Output Short-Circuit Duration . . . . . Indefinite  
 Di-Electrically Isolated PR40 Process . . . . . Latch-up free  
 ESD Rating  
   Human Body Model (Tested per JESD22-A114F) . . . . . 4kV  
   Machine Model (Tested per EIA/JESD22-A115-A) . . . . . 200V  
   Charged Device Model (Tested per JESD22-C101D) . . . . . 1.5kV

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
5 Ld SOT-23 (Notes 5, 6) . . . . .	190	90
6 Ld SOT-23 (Notes 5, 6) . . . . .	180	90
Maximum Storage Temperature Range . . .	-65 $^{\circ}C$ to +150 $^{\circ}C$	
Maximum Junction Temperature ( $T_{JMAX}$ ) . . . . .	+150 $^{\circ}C$	
Pb-Free Reflow Profile . . . . .	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

## Recommended Operating Conditions

Ambient Temperature Range ( $T_A$ ) . . . . . -40 $^{\circ}C$  to +125 $^{\circ}C$

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

### NOTES:

5.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**Electrical Specifications**  $V_{CC} = 12V$ ,  $V_{RS+} = 0V$  to 28V,  $V_{SENSE} = 0V$ ,  $R_{LOAD} = 1M\Omega$ ,  $T_A = +25^{\circ}C$  unless otherwise specified.  
**Boldface limits apply over the operating temperature range, -40 $^{\circ}C$  to +125 $^{\circ}C$ .**  
**Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OS}$ (Input Offset Voltage)	Gain = 100 (Notes 8, 9)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to 100mV	-250	60	250	$\mu V$
		<b>-300</b>		<b>300</b>	$\mu V$	
	$V_{CC} = 12V$ , $V_{RS+} = 0.2V$ , $V_{SENSE} = 20mV$ to 100mV	-2.5	-1.2	2.5	mV	
		<b>-2.8</b>		<b>2.8</b>	mV	
	Gain = 50, Gain = 20 (Notes 8, 9)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to 100mV	-300	60	300	$\mu V$
		<b>-450</b>		<b>450</b>	$\mu V$	
$V_{CC} = 12V$ , $V_{RS+} = 0.2V$ , $V_{SENSE} = 20mV$ to 100mV	-2.8	-1.2	2.8	mV		
	<b>-3.2</b>		<b>3.2</b>	mV		
Adjustable, Gain = 21 $R_f = 100k\Omega$ , $R_g = 5k\Omega$ (Notes 8, 9)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to 100mV	-300	60	300	$\mu V$	
	<b>-450</b>		<b>450</b>	$\mu V$		
	$V_{CC} = 12V$ , $V_{RS+} = 0.2V$ , $V_{SENSE} = 20mV$ to 100mV	-3.1	-1.2	3.1	mV	
		<b>-3.4</b>		<b>3.4</b>	mV	
$I_{RS+}$ , $I_{RS-}$	Leakage Current	$V_{CC} = 0V$ , $V_{RS+} = 28V$		0.041	1.2	$\mu A$
					<b>1.5</b>	$\mu A$

# ISL28006

**Electrical Specifications**  $V_{CC} = 12V$ ,  $V_{RS+} = 0V$  to  $28V$ ,  $V_{SENSE} = 0V$ ,  $R_{LOAD} = 1M\Omega$ ,  $T_A = +25^\circ C$  unless otherwise specified.  
**Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ .**  
**Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	
$I_{RS+}$ (+ Input Bias Current)	Gain = 100	$V_{RS+} = 2V$ , $V_{SENSE} = 5mV$		4.7	6	$\mu A$	
					<b>7</b>	$\mu A$	
		$V_{RS+} = 0V$ , $V_{SENSE} = 5mV$	-500	-432		nA	
			<b>-600</b>			nA	
	Gain = 50, Gain = 20	$V_{RS+} = 2V$ , $V_{SENSE} = 5mV$		4.7	6	$\mu A$	
					<b>8</b>	$\mu A$	
		$V_{RS+} = 0V$ , $V_{SENSE} = 5mV$	-700	-432		nA	
			<b>-840</b>			nA	
	ADJ Gain = 101 $R_f = 100k\Omega$ , $R_g = 1k\Omega$	$V_{RS+} = 2V$ , $V_{SENSE} = 5mV$		4.7	6	$\mu A$	
					<b>7</b>	$\mu A$	
		$V_{RS+} = 0V$ , $V_{SENSE} = 5mV$	-500	-432		nA	
			<b>-600</b>			nA	
$I_{RS-}$ (- Input Bias Current)	G = 100, 50, 20, ADJ	$V_{RS+} = 2V$ , $V_{SENSE} = 5mV$		5	50	nA	
					<b>75</b>	nA	
		$V_{RS+} = 0V$ , $V_{SENSE} = 5mV$	-125	-45		nA	
			<b>-130</b>			nA	
	CMRR	Common Mode Rejection Ratio	$V_{RS+} = 2V$ to $28V$	<b>105</b>	<b>115</b>		dB
	PSRR	Power Supply Rejection Ratio	$V_{CC} = 2.7V$ to $28V$ , $V_{RS+} = 2V$	<b>90</b>	<b>105</b>		dB
$V_{FS}$	Full-scale Sense Voltage	$V_{CC} = 28V$ , $V_{RS+} = 0.2V$ , $12V$	200			mV	
G (Gain)	(Note 8)	ISL28006-100		100		V/V	
		ISL28006-50		50		V/V	
		ISL28006-20		20		V/V	
		ISL28006-ADJ	20			V/V	
$G_A$ (Gain Accuracy)	Gain = 100 (Note 10)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to $100mV$	-0.2		0.7	%	
			<b>-1</b>		<b>1</b>	%	
		$V_{CC} = 12V$ , $V_{RS+} = 0.1V$ , $V_{SENSE} = 20mV$ to $100mV$		-0.25		%	
		Gain = 50, Gain = 20 (Note 10)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to $100mV$	-0.35		0.7	%
				<b>-1</b>		<b>1</b>	%
	$V_{CC} = 12V$ , $V_{RS+} = 0.1V$ , $V_{SENSE} = 20mV$ to $100mV$		-2.2	-0.33	2.2	%	
			<b>-2.3</b>		<b>2.3</b>	%	
	ADJ Gain = 21 $R_f = 100k\Omega$ , $R_g = 5k\Omega$ (Note 10)	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 20mV$ to $100mV$	-0.65		1	%	
			<b>-1</b>		<b>1.05</b>	%	
		$V_{CC} = 12V$ , $V_{RS+} = 0.1V$ , $V_{SENSE} = 20mV$ to $100mV$	-2.2	-0.33	2.2	%	
			<b>-2.3</b>		<b>2.3</b>	%	

# ISL28006

**Electrical Specifications**  $V_{CC} = 12V$ ,  $V_{RS+} = 0V$  to  $28V$ ,  $V_{SENSE} = 0V$ ,  $R_{LOAD} = 1M\Omega$ ,  $T_A = +25^\circ C$  unless otherwise specified.  
**Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ .**  
**Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V <sub>OA</sub> (Total Output Accuracy)	Gain = 100 (Note 11)	V <sub>CC</sub> = V <sub>RS+</sub> = 12V, V <sub>SENSE</sub> = 100mV	-0.7		0.7	%
			<b>-0.9</b>		<b>0.9</b>	%
		V <sub>CC</sub> = 12V, V <sub>RS+</sub> = 0.1V, V <sub>SENSE</sub> = 100mV		-1.25		%
	Gain = 50, Gain = 20 (Note 11)	V <sub>CC</sub> = V <sub>RS+</sub> = 12V, V <sub>SENSE</sub> = 100mV	-0.7		0.7	%
			<b>-0.9</b>		<b>0.9</b>	%
		V <sub>CC</sub> = 12V, V <sub>RS+</sub> = 0.1V, V <sub>SENSE</sub> = 100mV	-4.7	-1.41	1.8	%
		<b>-5.2</b>		<b>2.3</b>	%	
ADJ Gain = 21 R <sub>f</sub> = 100kΩ, R <sub>g</sub> = 5kΩ (Note 11)	V <sub>CC</sub> = V <sub>RS+</sub> = 12V, V <sub>SENSE</sub> = 100mV	-0.7		1.05	%	
		<b>-0.9</b>		<b>1.2</b>	%	
	V <sub>CC</sub> = 12V, V <sub>RS+</sub> = 0.1V, V <sub>SENSE</sub> = 100mV	-4.7	-1.41	1.8	%	
		<b>-5.2</b>		<b>2.3</b>	%	
V <sub>OH</sub>	Output Voltage Swing, High V <sub>CC</sub> - V <sub>OUT</sub>	I <sub>O</sub> = -500μA, V <sub>CC</sub> = 2.7V, V <sub>SENSE</sub> = 100mV, V <sub>RS+</sub> = 2V		39	50	mV
V <sub>OL</sub>	Output Voltage Swing, Low V <sub>OUT</sub>	I <sub>O</sub> = 500μA, V <sub>CC</sub> = 2.7V V <sub>SENSE</sub> = 0V, V <sub>RS+</sub> = 2V		30	50	mV
R <sub>OUT</sub>	Output Resistance	V <sub>CC</sub> = V <sub>RS+</sub> = 12V, V <sub>SENSE</sub> = 100mV I <sub>OUT</sub> = 10μA to 1mA		6.5		Ω
I <sub>SC+</sub>	Short Circuit Sourcing Current	V <sub>CC</sub> = V <sub>RS+</sub> = 5V, R <sub>L</sub> = 10Ω		4.8		mA
I <sub>SC-</sub>	Short Circuit Sinking Current	V <sub>CC</sub> = V <sub>RS+</sub> = 5V, R <sub>L</sub> = 10Ω		8.7		mA
I <sub>S</sub>	Gain = 100	V <sub>RS+</sub> > 2V, V <sub>SENSE</sub> = 5mV		50	59	μA
					<b>62</b>	μA
	Gain = 50, 20,	V <sub>RS+</sub> > 2V, V <sub>SENSE</sub> = 5mV		50	62	μA
					<b>63</b>	μA
	ADJ Gain = 21 R <sub>f</sub> = 100kΩ, R <sub>g</sub> = 5kΩ	V <sub>RS+</sub> > 2V, V <sub>SENSE</sub> = 5mV		50	62	μA
					<b>63</b>	μA
V <sub>CC</sub>	Supply Voltage	Guaranteed by PSRR	<b>2.7</b>		<b>28</b>	V
Slew Rate	Gain = 100	Pulse on R <sub>S+</sub> pin, V <sub>OUT</sub> = 8V <sub>p-p</sub> (Figure 65)	0.58	0.76		V/μs
	Gain = 50	Pulse on R <sub>S+</sub> pin, V <sub>OUT</sub> = 8V <sub>p-p</sub> (Figure 65)	0.58	0.67		V/μs
	Gain = 20	Pulse on R <sub>S+</sub> pin, V <sub>OUT</sub> = 3.5V <sub>p-p</sub> (Figure 65)	0.50	0.67		V/μs
	ADJ Gain = 21 R <sub>f</sub> = 100kΩ, R <sub>g</sub> = 5kΩ	Pulse on R <sub>S+</sub> pin, V <sub>OUT</sub> = 3.5V <sub>p-p</sub> (Figure 65)	0.50	0.67		V/μs

# ISL28006

**Electrical Specifications**  $V_{CC} = 12V$ ,  $V_{RS+} = 0V$  to  $28V$ ,  $V_{SENSE} = 0V$ ,  $R_{LOAD} = 1M\Omega$ ,  $T_A = +25^\circ C$  unless otherwise specified.  
**Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ .**  
**Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
BW-3dB	Gain = 100	$V_{RS+} = 12V$ , $0.1V$ , $V_{SENSE} = 100mV$		110		kHz
	Gain = 50	$V_{RS+} = 12V$ , $0.1V$ , $V_{SENSE} = 100mV$		160		kHz
	Gain = 20	$V_{RS+} = 12V$ , $0.1V$ , $V_{SENSE} = 100mV$		180		kHz
	ADJ, Gain = 101 (Figure 57)	$V_{RS+} = 12V$ , $0.1V$ , $V_{SENSE} = 100mV$ , $R_f = 100k\Omega$ , $R_g = 1k\Omega$		40		kHz
	ADJ, Gain = 51 (Figure 57)	$V_{RS+} = 12V$ , $V_{SENSE} = 100mV$ , $R_f = 100k\Omega$ , $R_g = 2k\Omega$		78		kHz
		$V_{RS+} = 0.1V$ , $V_{SENSE} = 100mV$ , $R_f = 100k\Omega$ , $R_g = 2k\Omega$		122		kHz
	ADJ, Gain = 21 (Figure 57)	$V_{RS+} = 12V$ , $V_{SENSE} = 100mV$ , $R_f = 100k\Omega$ , $R_g = 5k\Omega$		131		kHz
$V_{RS+} = 0.1V$ , $V_{SENSE} = 100mV$ , $R_f = 100k\Omega$ , $R_g = 5k\Omega$			237		kHz	
$t_s$	Output Settling Time to 1% of Final Value	$V_{CC} = V_{RS+} = 12V$ , $V_{OUT} = 10V$ step, $V_{SENSE} > 7mV$		15		$\mu s$
		$V_{CC} = V_{RS+} = 0.2V$ , $V_{OUT} = 10V$ step, $V_{SENSE} > 7mV$		20		$\mu s$
	Capacitive-Load Stability	No sustained oscillations		300		pF
$t_s$ Power-up	Power-Up Time to 1% of Final Value	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 100mV$		15		$\mu s$
		$V_{CC} = 12V$ , $V_{RS+} = 0.2V$ , $V_{SENSE} = 100mV$		50		$\mu s$
	Saturation Recovery Time	$V_{CC} = V_{RS+} = 12V$ , $V_{SENSE} = 100mV$ , overdrive		10		$\mu s$

**NOTES:**

7. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

**8. DEFINITION OF TERMS:**

- $V_{SENSE A} = V_{SENSE} @ 100mV$
- $V_{SENSE B} = V_{SENSE} @ 20mV$
- $V_{OUT A} = V_{OUT} @ V_{SENSE A} = 100mV$
- $V_{OUT B} = V_{OUT} @ V_{SENSE B} = 20mV$

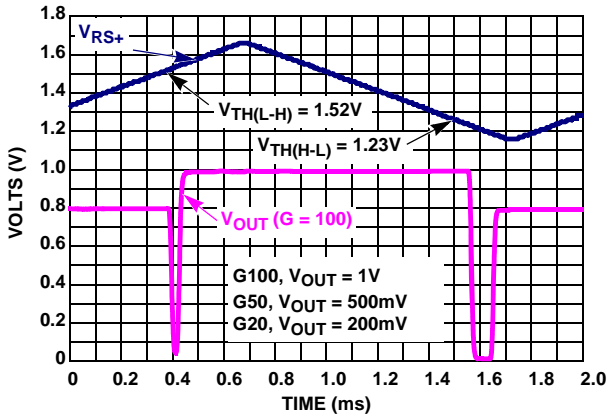
$$G = \text{GAIN} = \left( \frac{V_{OUT A} - V_{OUT B}}{V_{SENSE A} - V_{SENSE B}} \right)$$

9.  $V_{OS}$  is extrapolated from the gain measurement.  $V_{OS} = V_{SENSE A} - \frac{V_{OUT A}}{G}$

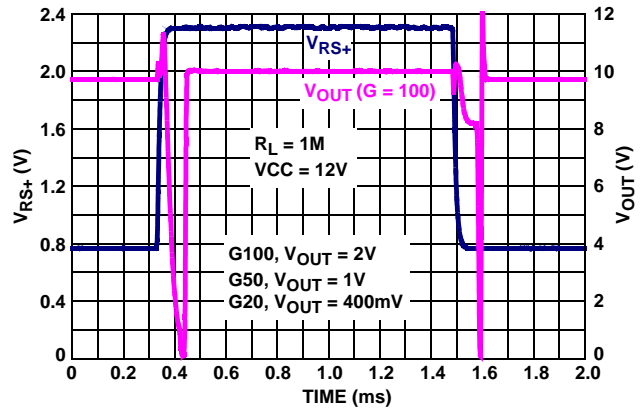
$$10. \% \text{ Gain Accuracy} = G_A = \left( \frac{G_{MEASURED} - G_{EXPECTED}}{G_{EXPECTED}} \right) \times 100$$

$$11. \text{ Output Accuracy \% VOA} = \left( \frac{V_{OUT MEASURED} - V_{OUT EXPECTED}}{V_{OUT EXPECTED}} \right) \times 100 \text{ where } V_{OUT} = V_{SENSE} \times \text{GAIN and } V_{SENSE} = 100mV$$

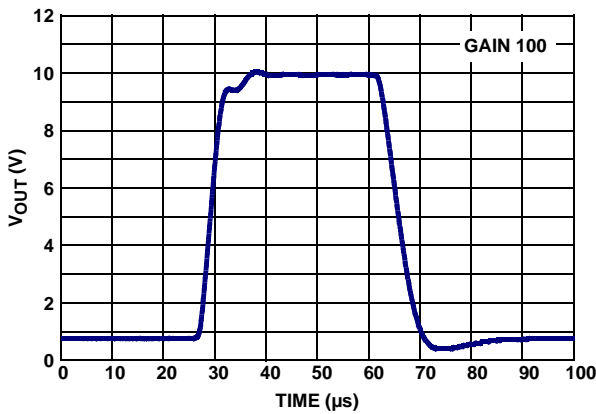
**Typical Performance Curves**  $V_{CC} = 12V, R_L = 1M$ , unless otherwise specified.



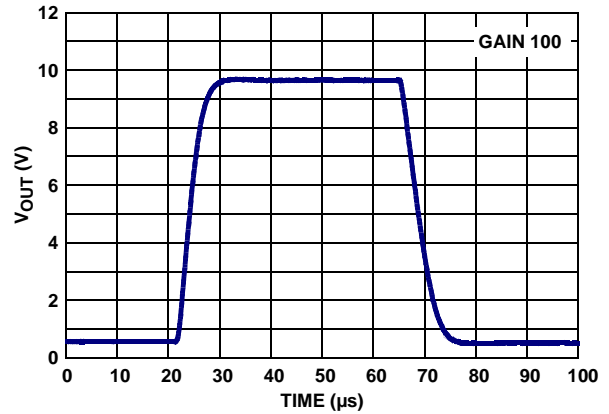
**FIGURE 1. HIGH-SIDE and LOW-SIDE THRESHOLD VOLTAGE  $V_{RS+(L-H)}$  and  $V_{RS+(H-L)}$ ,  $V_{SENSE} = 10mV$**



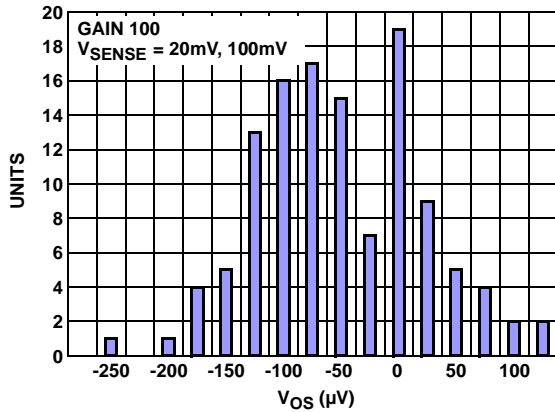
**FIGURE 2.  $V_{OUT}$  vs  $V_{RS+}$ ,  $V_{SENSE} = 20mV$  TRANSIENT RESPONSE**



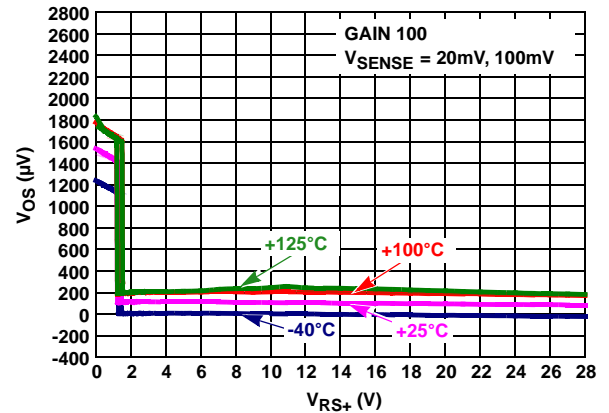
**FIGURE 3. LARGE SIGNAL TRANSIENT RESPONSE  $V_{RS+} = 0.2V, V_{SENSE} = 100mV$**



**FIGURE 4. LARGE SIGNAL TRANSIENT RESPONSE  $V_{RS+} = 12V, V_{SENSE} = 100mV$**



**FIGURE 5.  $V_{OS}$  ( $\mu V$ ) DISTRIBUTION AT  $+25^\circ C$ ,  $V_{RS+} = 12V$ , QUANTITY: 100**



**FIGURE 6.  $V_{OS}$  vs  $V_{RS+}$**

Typical Performance Curves  $V_{CC} = 12V, R_L = 1M$ , unless otherwise specified. (Continued)

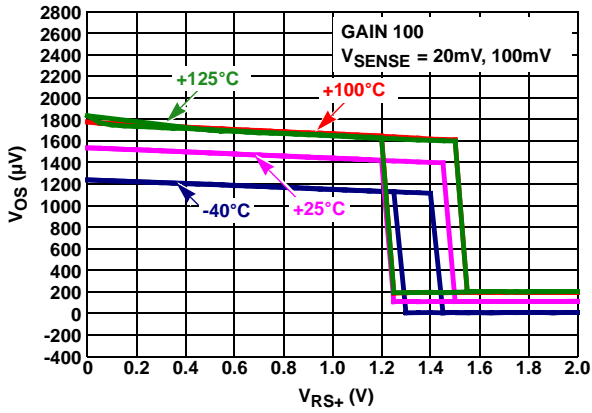


FIGURE 7.  $V_{OS}$  vs  $V_{RS+}$

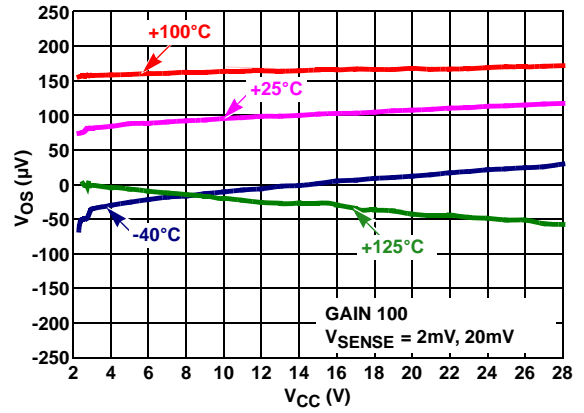


FIGURE 8.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = 12V$

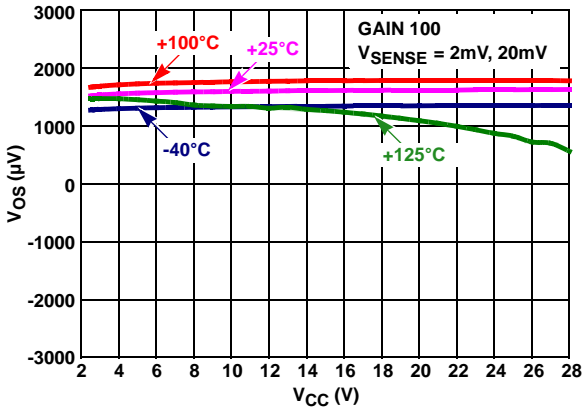


FIGURE 9.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = 0.1V$

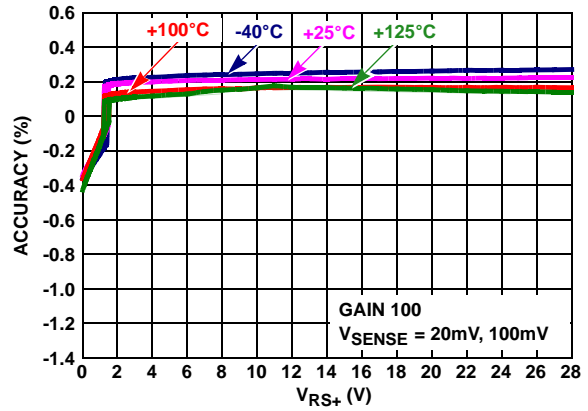


FIGURE 10. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $28V$

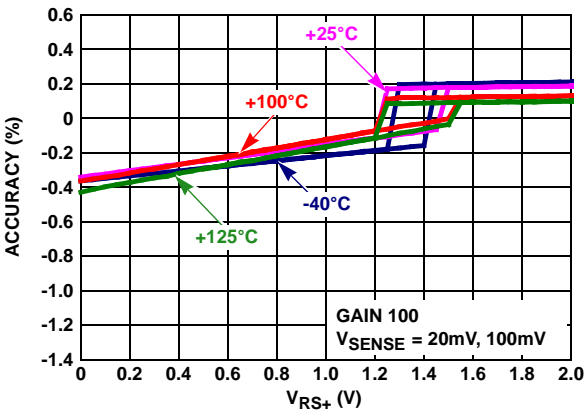


FIGURE 11. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $2V$

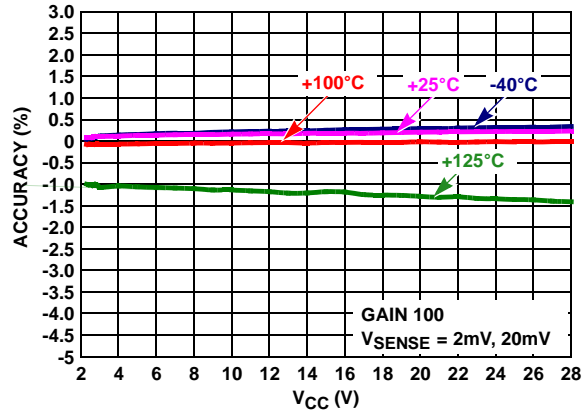


FIGURE 12. GAIN ACCURACY vs  $V_{CC}$ ,  $V_{RS+} = 12V$

**Typical Performance Curves**  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

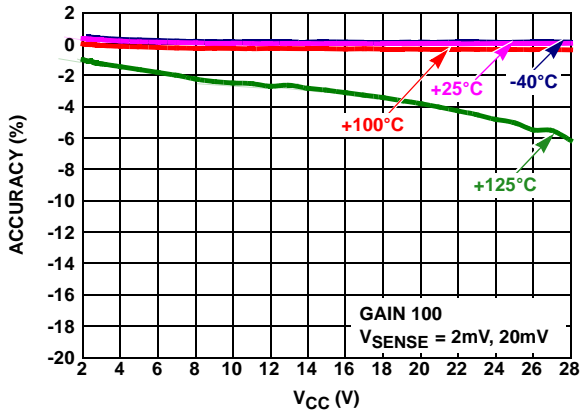


FIGURE 13. GAIN ACCURACY vs  $V_{CC}$ ,  $V_{RS+} = 0.1V$

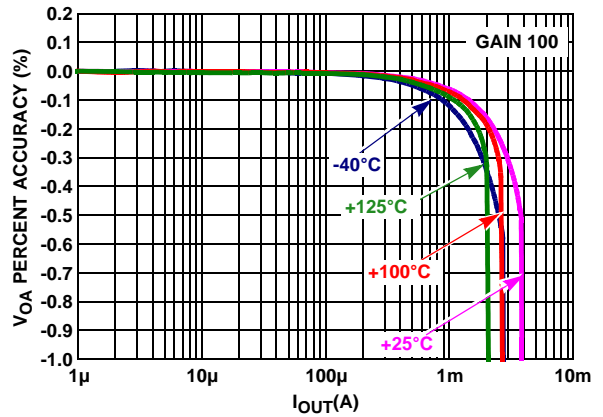


FIGURE 14. NORMALIZED  $V_{OA}$  vs  $I_{OUT}$

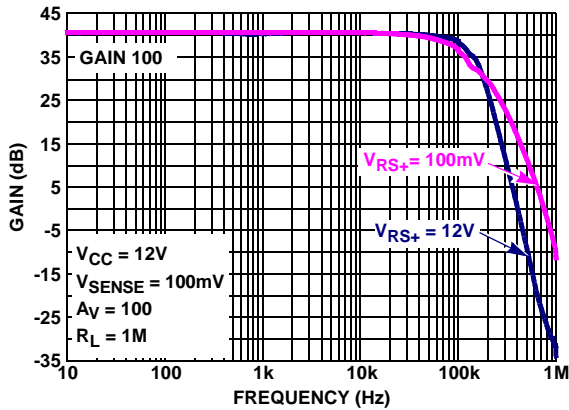


FIGURE 15. GAIN vs FREQUENCY  $V_{RS+} = 100mV/12V$ ,  $V_{SENSE} = 100mV$ ,  $V_{OUT} = 50mV_{p-p}$

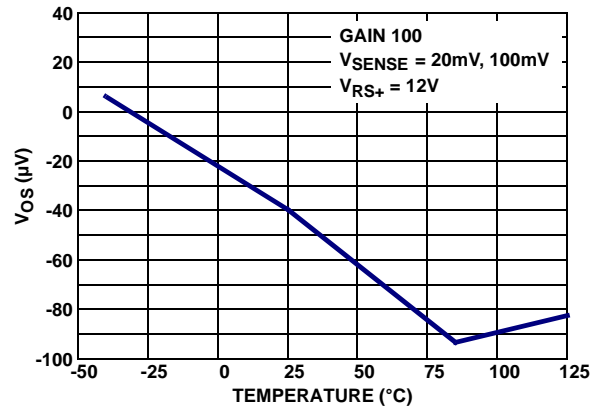


FIGURE 16.  $V_{OS}$  ( $\mu V$ ) vs TEMPERATURE

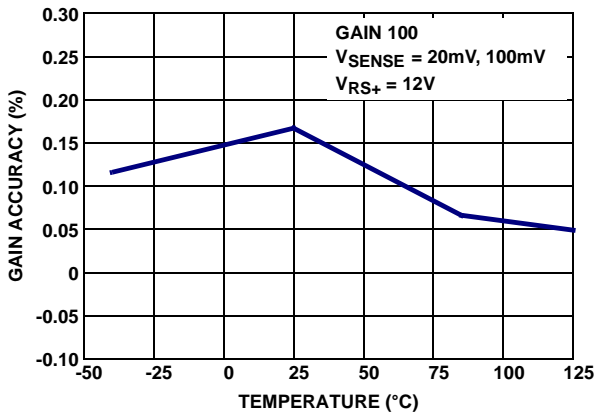


FIGURE 17. GAIN ACCURACY (%) vs TEMPERATURE

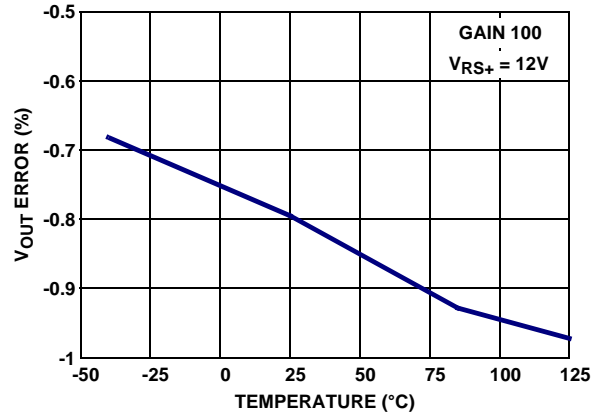


FIGURE 18.  $V_{OUT}$  ERROR (%) vs TEMPERATURE

Typical Performance Curves  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

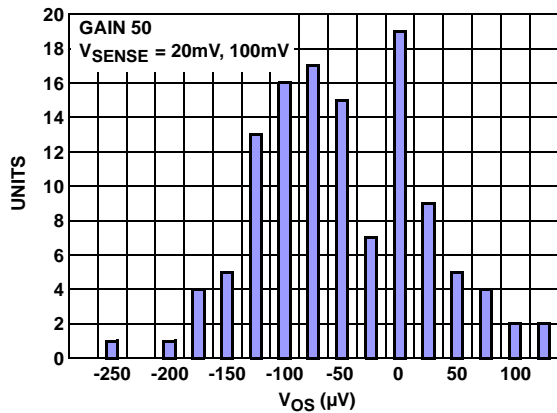


FIGURE 19.  $V_{OS}$  ( $\mu V$ ) DISTRIBUTION AT  $+25^{\circ}C$ ,  $V_{RS+} = 12V$ , QUANTITY: 100

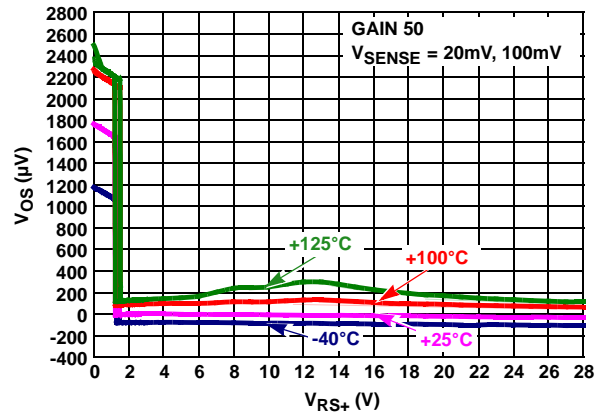


FIGURE 20.  $V_{OS}$  vs  $V_{RS+}$

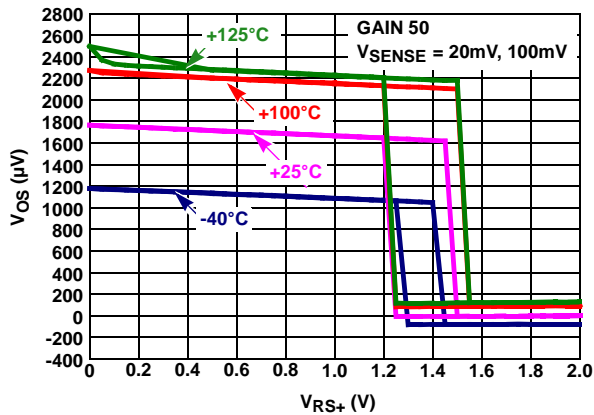


FIGURE 21.  $V_{OS}$  vs  $V_{RS+}$

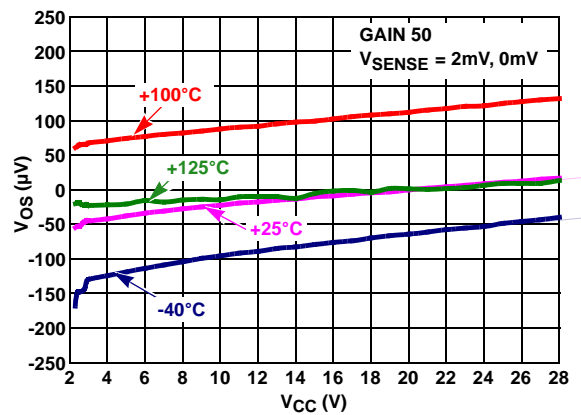


FIGURE 22.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = 12V$

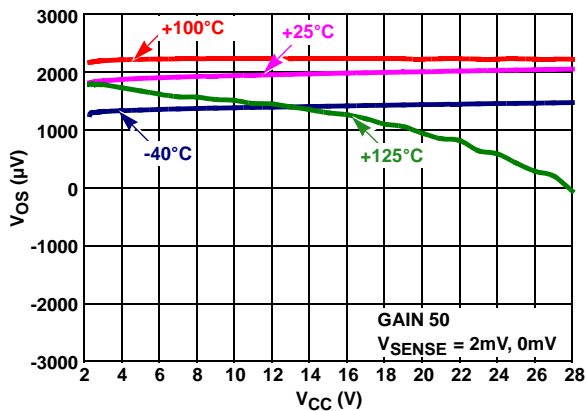


FIGURE 23.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = V_{RS+} = 0.1V$

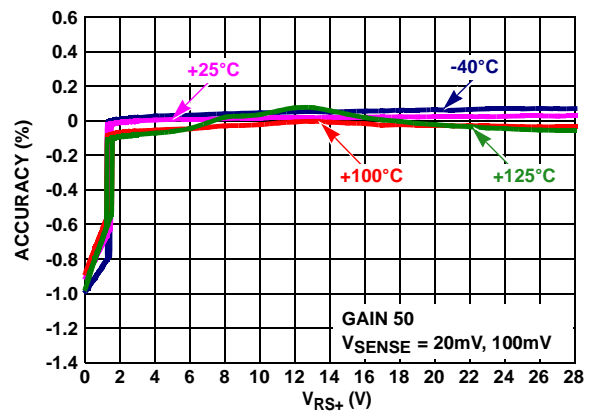


FIGURE 24. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $28V$

**Typical Performance Curves**  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

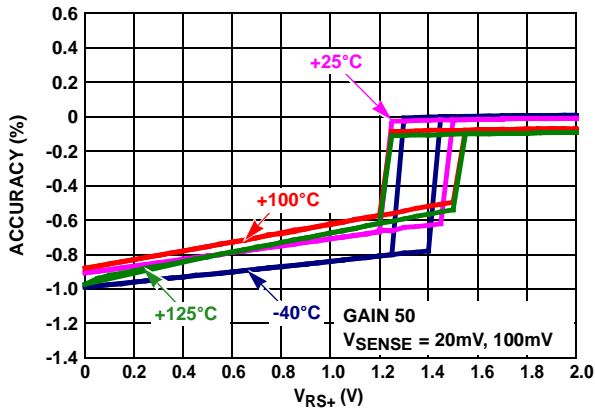


FIGURE 25. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $2V$

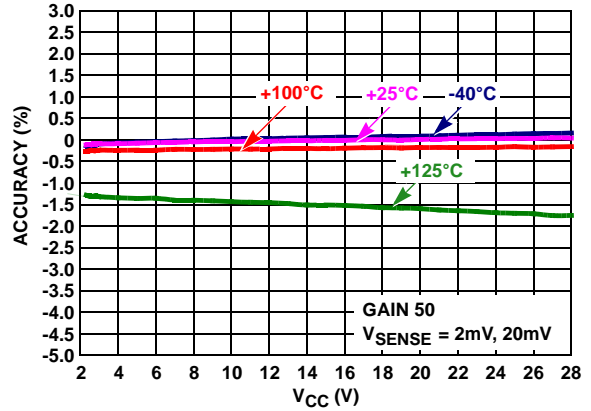


FIGURE 26. GAIN ACCURACY vs  $V_{CC}$ , HIGH-SIDE

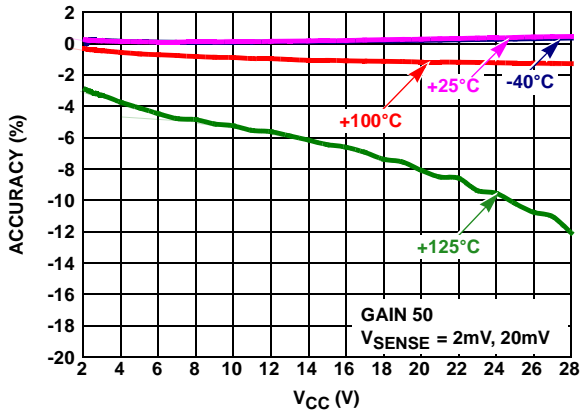


FIGURE 27. GAIN ACCURACY vs  $V_{CC}$ , LOW-SIDE

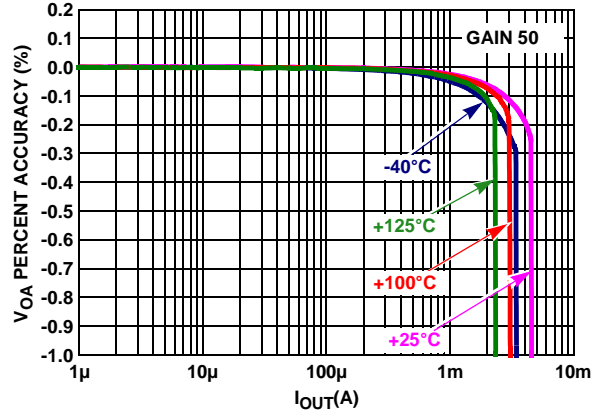


FIGURE 28. NORMALIZED  $V_{OA}$  vs  $I_{OUT}$

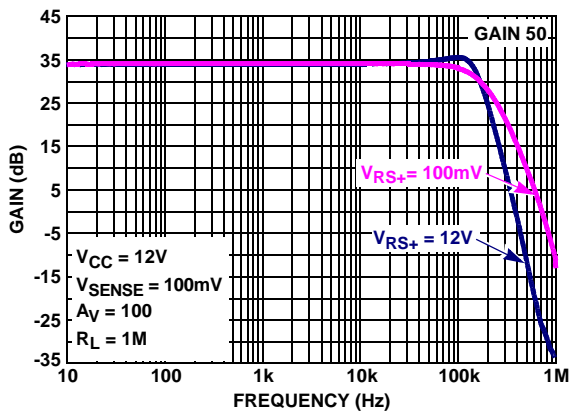


FIGURE 29. GAIN vs FREQUENCY  $V_{RS+} = 100mV/12V$ ,  $V_{SENSE} = 100mV$ ,  $V_{OUT} = 50mV_{p-p}$

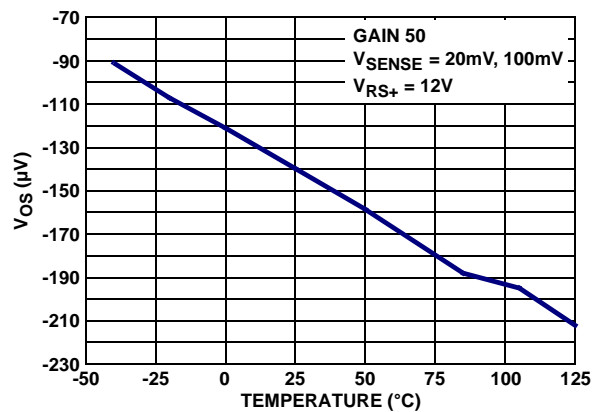


FIGURE 30.  $V_{OS}$  ( $\mu V$ ) vs TEMPERATURE

**Typical Performance Curves**  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

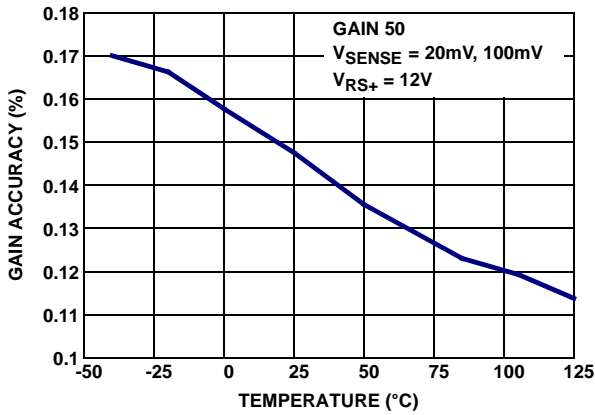


FIGURE 31. GAIN ACCURACY (%) vs TEMPERATURE

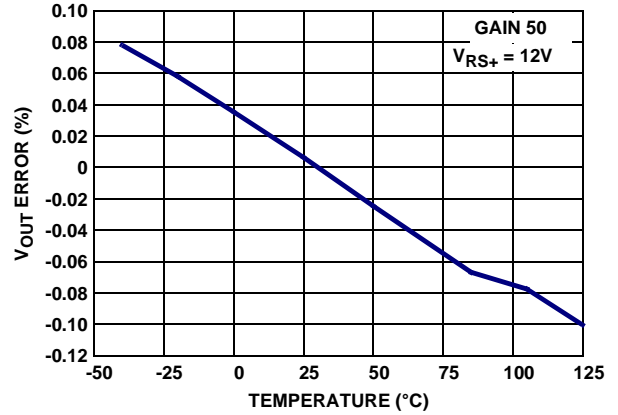


FIGURE 32.  $V_{OUT}$  ERROR (%) vs TEMPERATURE

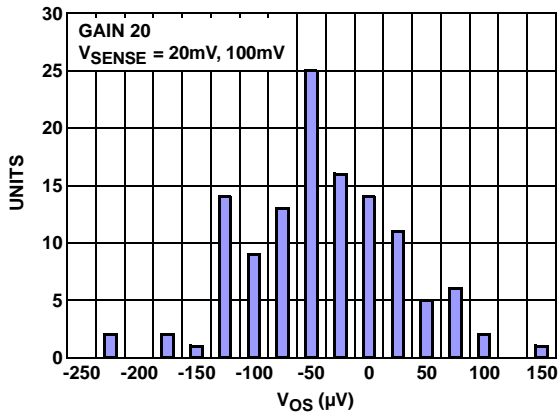


FIGURE 33.  $V_{OS}$  (µV) DISTRIBUTION AT +25°C,  $V_{RS+} = 12V$ , QUANTITY: 100

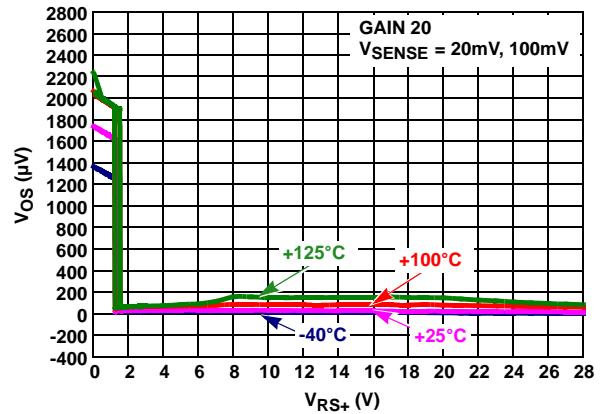


FIGURE 34.  $V_{OS}$  vs  $V_{RS+}$

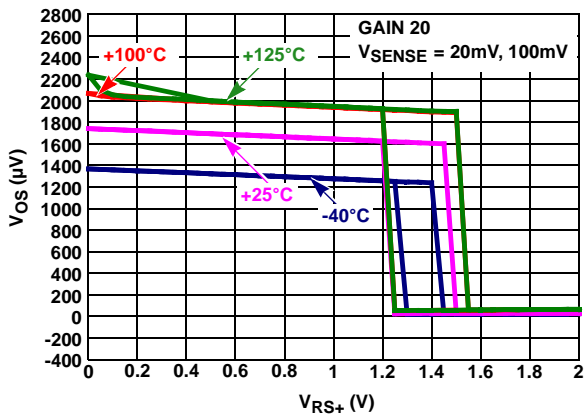


FIGURE 35.  $V_{OS}$  vs  $V_{RS+}$

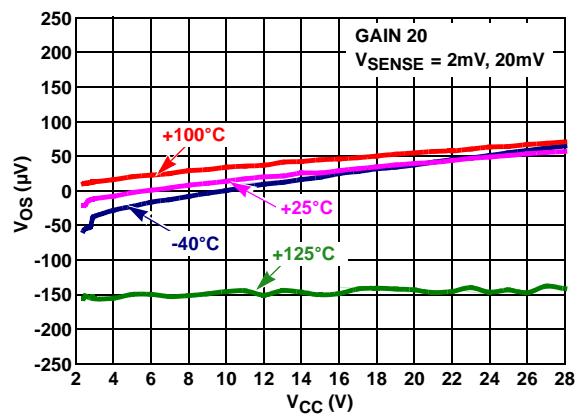


FIGURE 36.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = 12V$

Typical Performance Curves  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

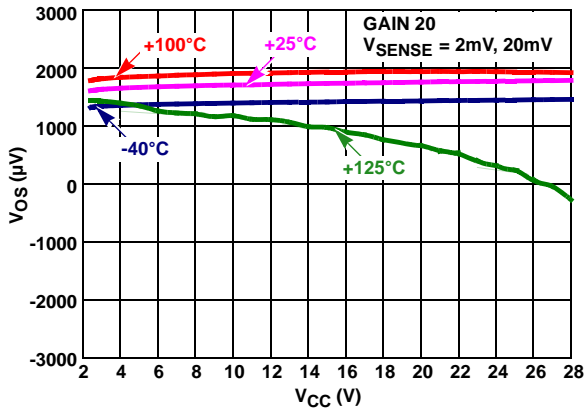


FIGURE 37.  $V_{OS}$  vs  $V_{CC}$ ,  $V_{RS+} = 0.1V$

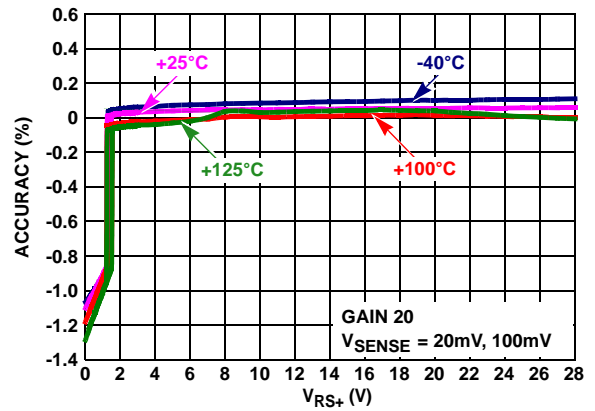


FIGURE 38. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $28V$

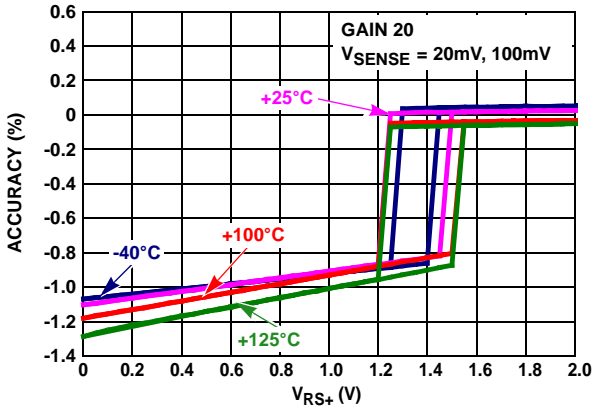


FIGURE 39. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $2V$

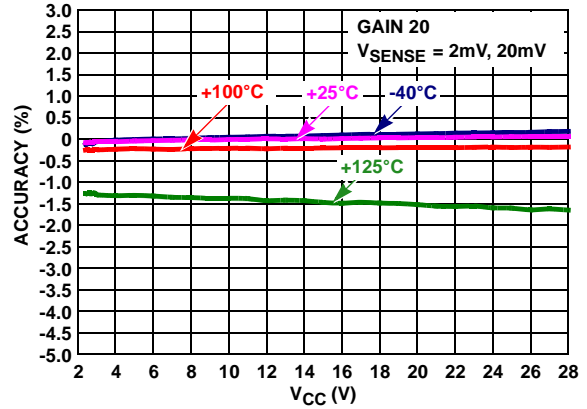


FIGURE 40. GAIN ACCURACY vs  $V_{CC}$ , HIGH-SIDE

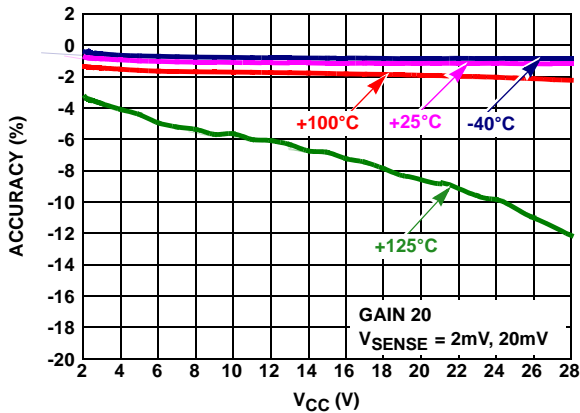


FIGURE 41. GAIN ACCURACY vs  $V_{CC}$ , LOW-SIDE

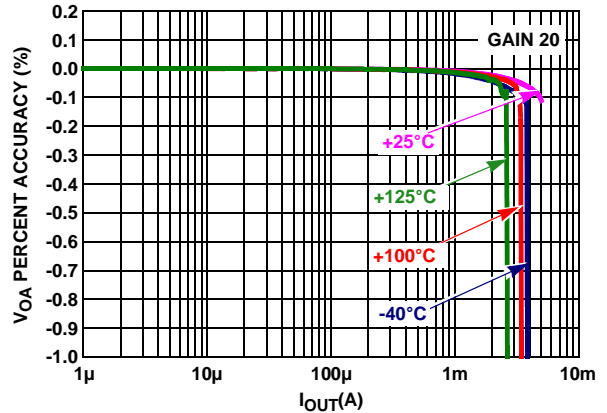


FIGURE 42. NORMALIZED  $V_{OA}$  vs  $I_{OUT}$

Typical Performance Curves  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

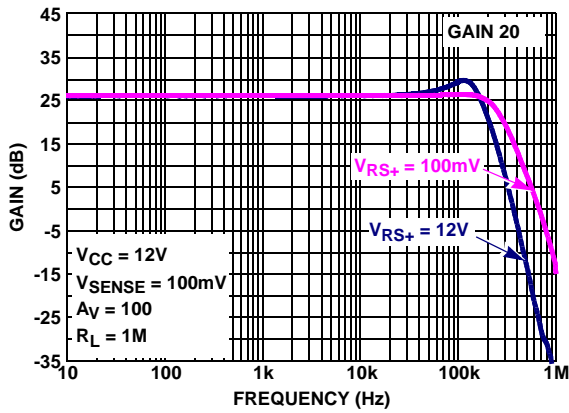


FIGURE 43. GAIN vs FREQUENCY  $V_{RS+} = 100mV/12V$ ,  $V_{SENSE} = 100mV$ ,  $V_{OUT} = 50mV_{p-p}$

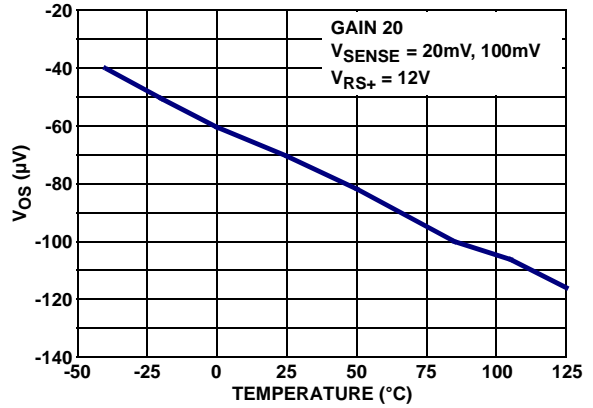


FIGURE 44.  $V_{OS}$  ( $\mu V$ ) vs TEMPERATURE

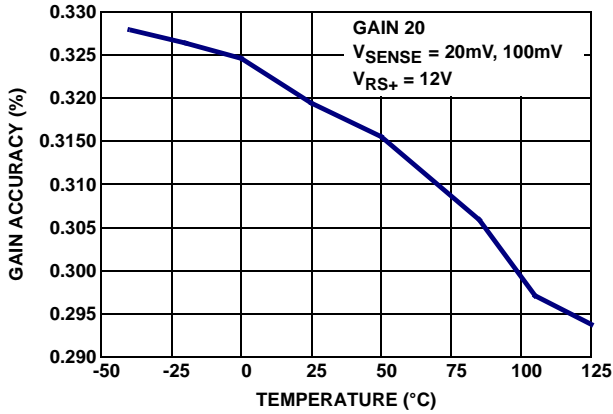


FIGURE 45. GAIN ACCURACY (%) vs TEMPERATURE

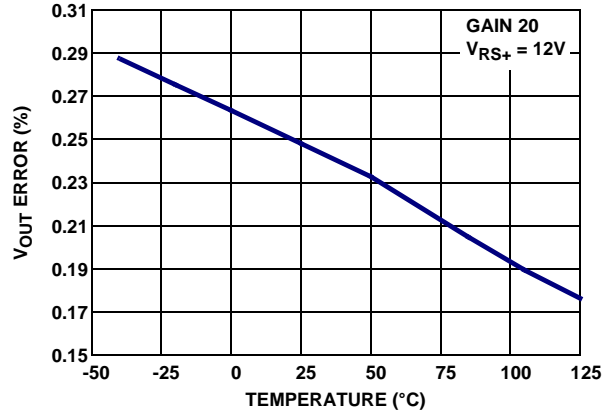


FIGURE 46.  $V_{OUT}$  ERROR (%) vs TEMPERATURE

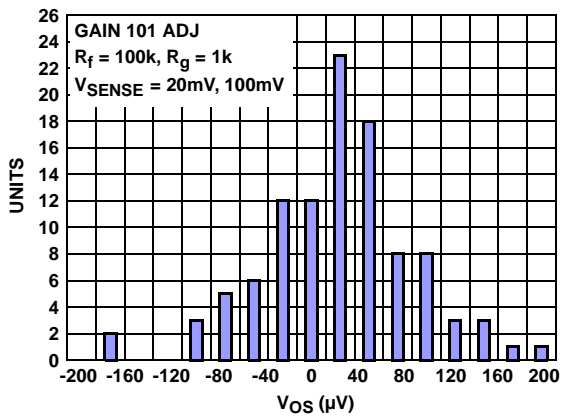


FIGURE 47.  $V_{OS}$  ( $\mu V$ ) DISTRIBUTION AT  $+25^{\circ}C$ ,  $V_{RS+} = 12V$ , QUANTITY: 100

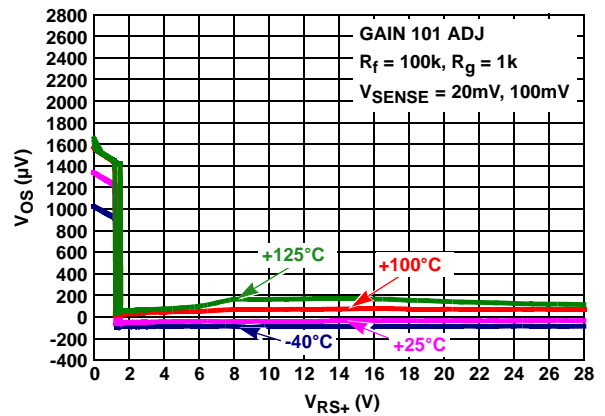


FIGURE 48.  $V_{OS}$  vs  $V_{RS+}$

Typical Performance Curves  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

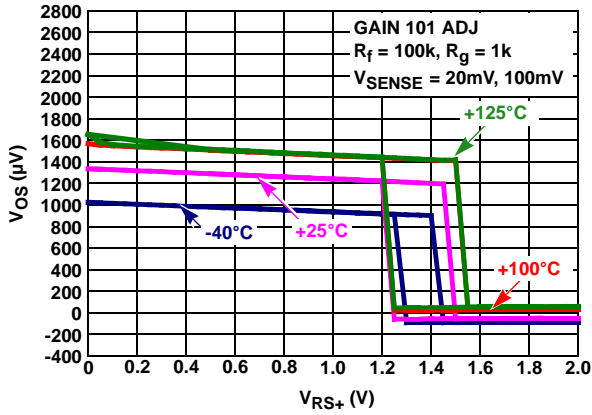


FIGURE 49.  $V_{OS}$  vs  $V_{RS+}$

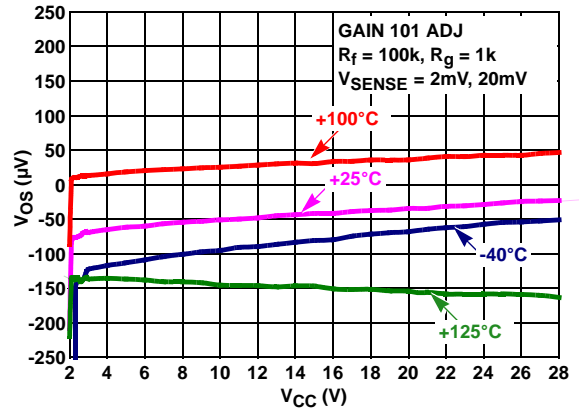


FIGURE 50.  $V_{OS}$  vs  $V_{CC}$ , HIGH-SIDE

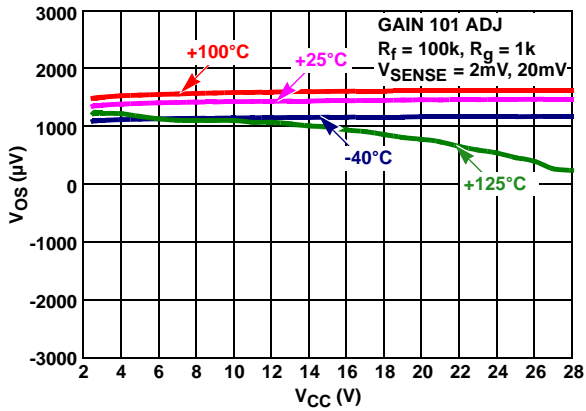


FIGURE 51.  $V_{OS}$  vs  $V_{CC}$ , LOW-SIDE

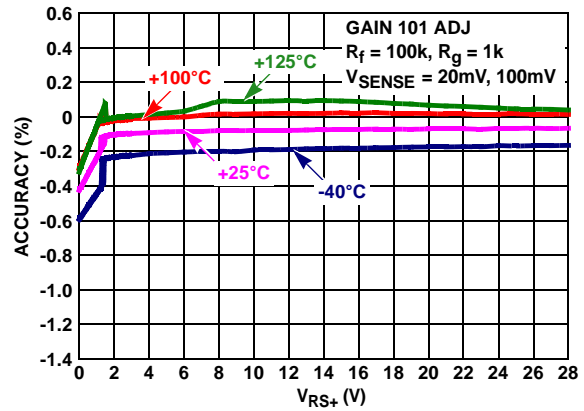


FIGURE 52. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $28V$

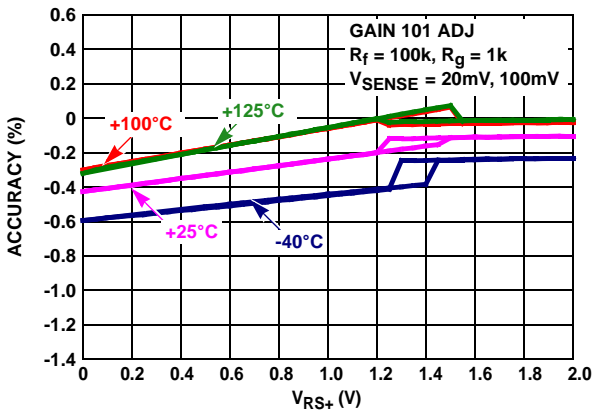


FIGURE 53. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $2V$

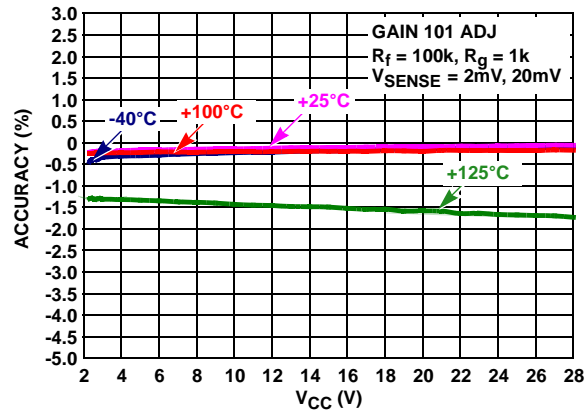


FIGURE 54. GAIN ACCURACY vs  $V_{CC}$ ,  $V_{RS+} = 12V$

Typical Performance Curves  $V_{CC} = 12V$ ,  $R_L = 1M$ , unless otherwise specified. (Continued)

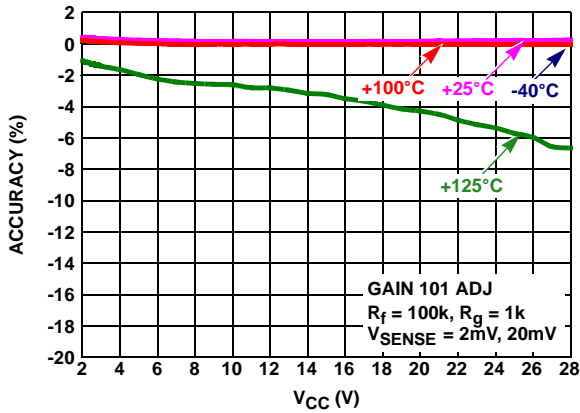


FIGURE 55. GAIN ACCURACY vs  $V_{CC}$ ,  $V_{RS+} = 0.1V$

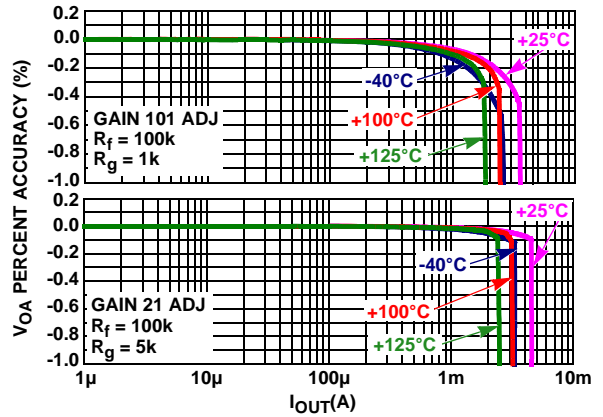


FIGURE 56. NORMALIZED  $V_{OA}$  vs  $I_{OUT}$

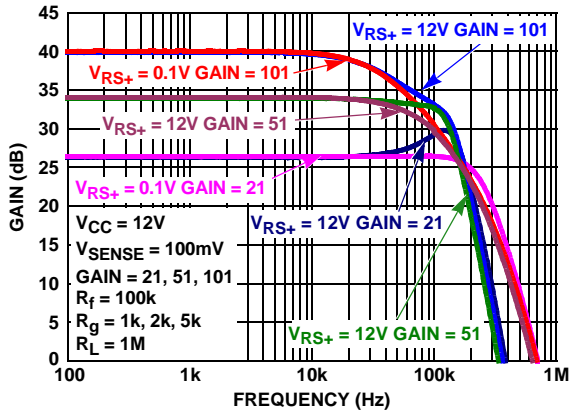


FIGURE 57. GAIN vs FREQUENCY  $V_{RS+} = 100mV/12V$ ,  $V_{SENSE} = 100mV$ ,  $V_{OUT} = 50mV_{p-p}$

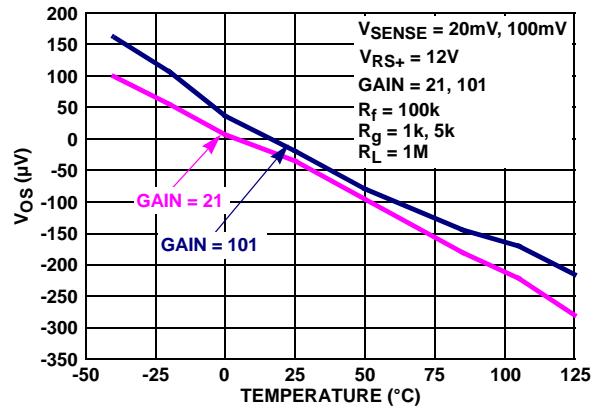


FIGURE 58.  $V_{OS}$  ( $\mu V$ ) vs TEMPERATURE

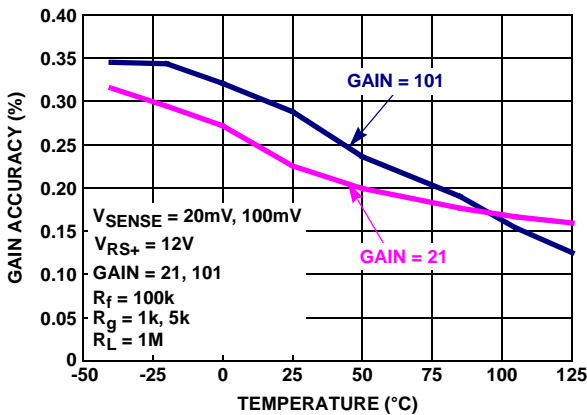


FIGURE 59. GAIN ACCURACY (%) vs TEMPERATURE

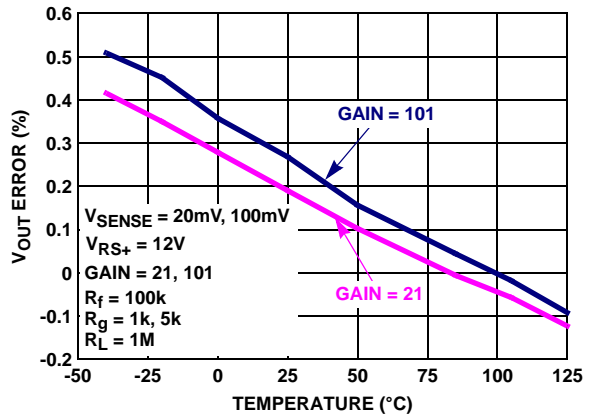


FIGURE 60.  $V_{OUT}$  ERROR (%) vs TEMPERATURE

## Test Circuits and Waveforms

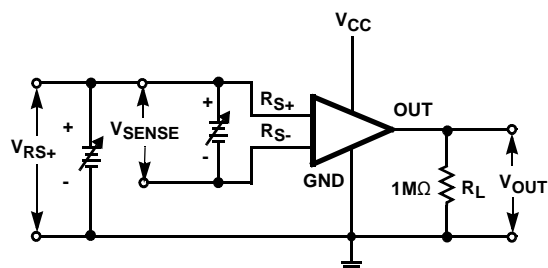


FIGURE 61.  $I_S$ ,  $V_{OS}$ ,  $V_{OA}$ ,  $CMRR$ ,  $PSRR$ ,  $GAIN$  ACCURACY

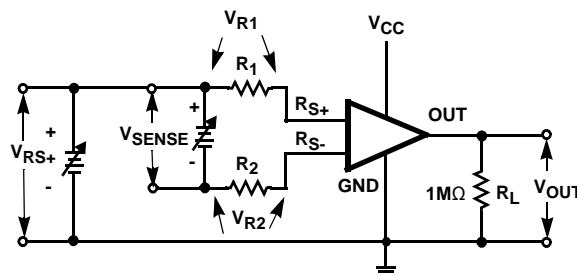


FIGURE 62.  $INPUT$  BIAS CURRENT,  $LEAKAGE$  CURRENT

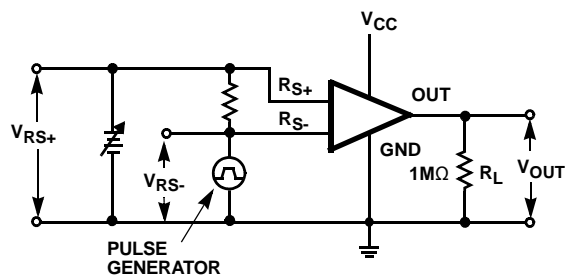


FIGURE 63.  $t_{sr}$ ,  $SATURATION$  RECOVERY TIME

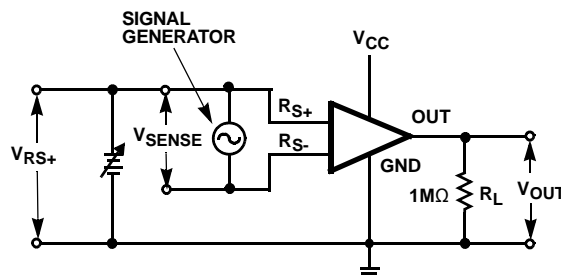


FIGURE 64.  $GAIN$  vs  $FREQUENCY$

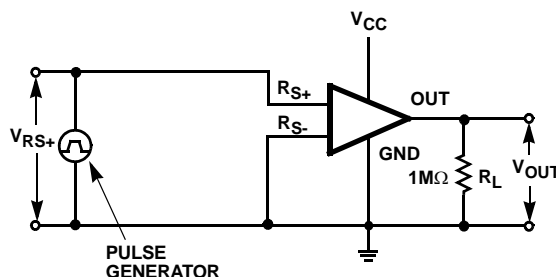


FIGURE 65.  $SLEW$  RATE

## Applications Information

### Functional Description

The ISL28006-20, ISL28006-50 and ISL28006-100 are single supply, uni-directional current sense amplifiers with fixed gains of 20V/V, 50V/V and 100V/V respectively. The ISL28006-ADJ is single supply, uni-directional current sense amplifier with an adjustable gain via external resistors (see Figure 70). The ISL28006-ADJ is stable for gains of 20 and higher.

The ISL28006 is a 2-stage amplifier. Figure 66 shows the active circuitry for high-side current sense applications where the sense voltage is between 1.35V to 28V. Figure 67 shows the active circuitry for ground sense applications where the sense voltage is between 0V to 1.35V.

The first stage is a bi-level trans-conductance amp and level translator. The gm stage converts the low voltage drop ( $V_{SENSE}$ ) sensed across an external milli-ohm sense resistor, to a current (@  $g_m = 21.3\mu A/V$ ). The trans-conductance amplifier forces a current through  $R_1$

resulting to a voltage drop across  $R_1$  that is equal to the sense voltage ( $V_{SENSE}$ ). The current through  $R_1$  is mirrored across  $R_5$  creating a ground-referenced voltage at the input of the second amplifier equal to  $V_{SENSE}$ .

The second stage is responsible for the overall gain and frequency response performance of the device. The fixed gains (20, 50, 100) are set with internal resistors  $R_f$  and  $R_g$ . The variable gain (ADJ) has an additional FB pin and uses external gain resistors to set the gain of the output. For the fixed gain amps the only external component needed is a current sense resistor (typically  $0.001\Omega$  to  $0.01\Omega$ , 1W to 2W).

The transfer function for the fixed gain parts is given in Equation 1.

$$V_{OUT} = GAIN \times (I_S R_S + V_{OS}) \quad (EQ. 1)$$

The transfer function for the adjustable gain part is given in Equation 2.

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) (I_S R_S + V_{OS}) \quad (EQ. 2)$$

# ISL28006

The input gm stage derives its  $\sim 2.86\mu\text{A}$  supply current from the input source through the  $R_{S+}$  terminal as long as the sensed voltage at the  $R_{S+}$  pin is  $>1.35\text{V}$  and the  $gm_{HI}$  amplifier is selected. When the sense voltage at

$R_{S+}$  drops below the  $1.35\text{V}$  threshold, the  $gm_{LO}$  amplifier kicks in and the  $gm_{LO}$  output current reverses, flowing out of the  $R_{S-}$  pin.

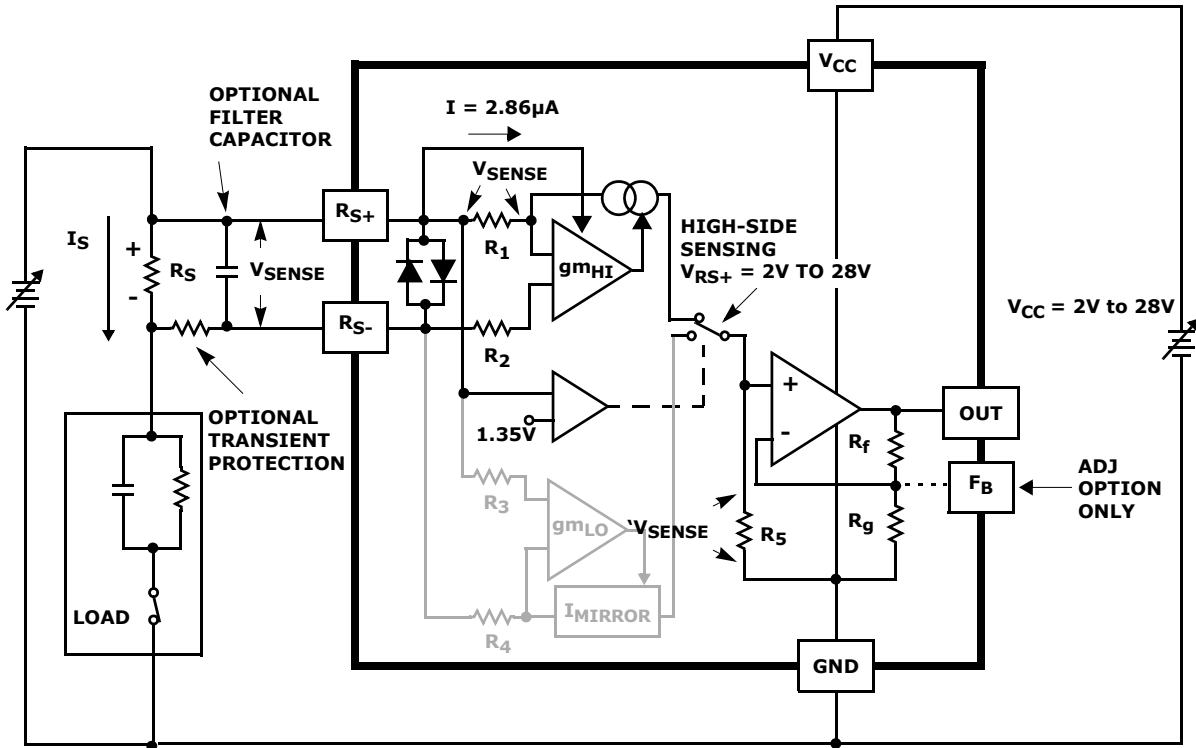


FIGURE 66. HIGH-SIDE CURRENT DETECTION

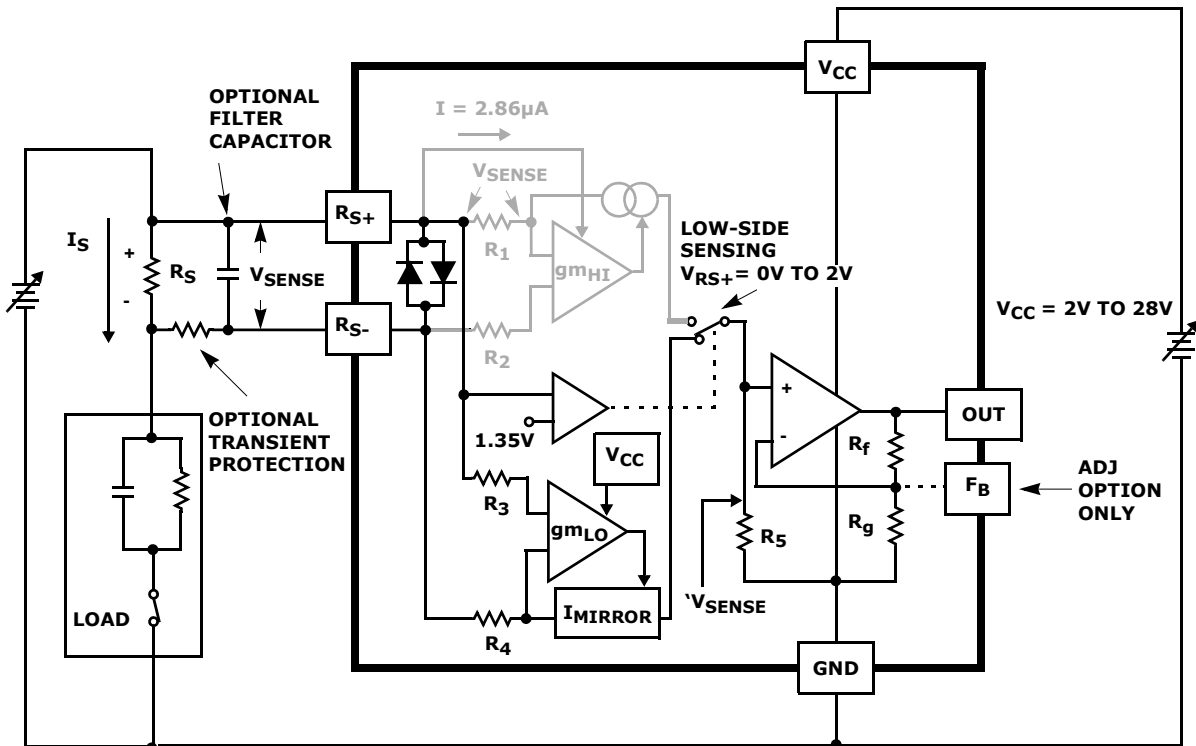


FIGURE 67. LOW-SIDE CURRENT SENSING DETECTION

### Hysteretic Comparator

The input trans-conductance amps are under control of a hysteretic comparator operating from the incoming source voltage on the  $R_{S+}$  pin (Figure 66). The comparator monitors the voltage on  $R_{S+}$  and switches the sense amplifier from the low-side gm amp to the high-side gm amplifier whenever the input voltage at  $R_{S+}$  increases above the 1.35V threshold. Conversely, a decreasing voltage on the  $R_{S+}$  pin, causes the hysteric comparator to switch from the high-side gm amp to the low-side gm amp as the voltage decreases below 1.35V. It is that low-side sense gm amplifier that gives the ISL28006 the proprietary ability to sense current all the way to 0V. Negative voltages on the  $R_{S+}$  or  $R_{S-}$  are beyond the sensing voltage range of this amplifier.

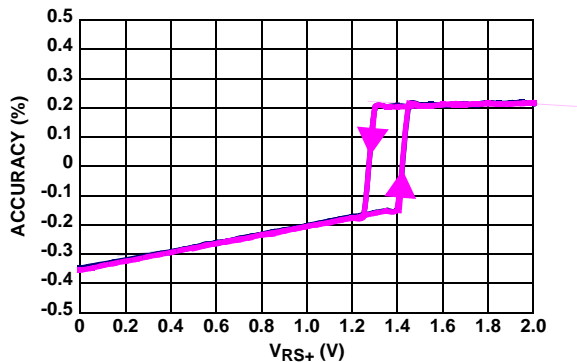


FIGURE 68. GAIN ACCURACY vs  $V_{RS+} = 0V$  TO  $2V$

### Typical Application Circuit

Figure 70 shows the basic application circuit and optional protection components for switched-load applications. For applications where the load and the power source is permanently connected, only an external sense resistor is needed. For applications where fast transients are caused by hot plugging the source or load, external protection components may be needed. The external current limiting resistor ( $R_P$ ) in Figure 70 may be required to limit the peak current through the internal ESD diodes to  $<20mA$ . This condition can occur in applications that experience high levels of in-rush current causing high peak voltages that can damage the internal ESD diodes. An  $R_P$  resistor value of  $100\Omega$  will provide

protection for a 2V transient with the maximum of 20mA flowing through the input while adding only an additional  $13\mu V$  (worse case over-temperature) of  $V_{OS}$ . Refer to Equation 3:

$$((R_P \times I_{RS-}) = (100\Omega \times 130nA) = 13\mu V) \tag{EQ. 3}$$

Switching applications can generate voltage spikes that can overdrive the amplifier input and drive the output of the amplifier into the rails, resulting in a long overload recover time. Capacitors  $C_M$  and  $C_D$  filter the common mode and differential voltage spikes.

### Error Sources

There are 3 dominant error sources: gain error, input offset voltage error and Kelvin voltage error (see Figure 69). The gain error is dominated by the internal resistance matching tolerances. The remaining errors appear as sense voltage errors at the input to the amplifier. They are  $V_{OS}$  of the amplifier and Kelvin voltage errors. If the transient protection resistor is added, an additional  $V_{OS}$  error can result from the  $I \times R$  voltage due to input bias current. The limiting resistor should only be added to the  $R_{S-}$  input, due to the high-side gm amplifier ( $gm_{HI}$ ) sinking several micro amps of current through the  $R_{S+}$  pin.

### Layout Guidelines

#### The Kelvin Connected Sense Resistor

The source of Kelvin voltage errors is illustrated in Figure 69. The resistance of 1/2 Oz copper is  $\sim 1m\Omega$  per square with a TC of  $\sim 3900ppm/^\circ C$  ( $0.39\%/^\circ C$ ). When you compare this unwanted parasitic resistance with the total  $1m\Omega$  to  $10m\Omega$  resistance of the sense resistor, it is easy to see why the sense connection must be chosen very carefully. For example, consider a maximum current of 20A through a  $0.005\Omega$  sense resistor, generating a  $V_{SENSE} = 0.1$  and a full scale output voltage of 10V ( $G = 100$ ). Two side contacts of only 0.25 square per contact puts the  $V_{SENSE}$  input about  $0.5 \times 1m\Omega$  away from the resistor end capacitor. If only 10A the 20A total current flows through the kelvin path to the resistor, you get an error voltage of 10mV ( $10A \times 0.5sq \times 0.001\Omega/sq = 10mV$ ) added to the 100mV sense voltage for a sense voltage error of 10%  $(0.110V-0.1)/0.1V \times 100$ .

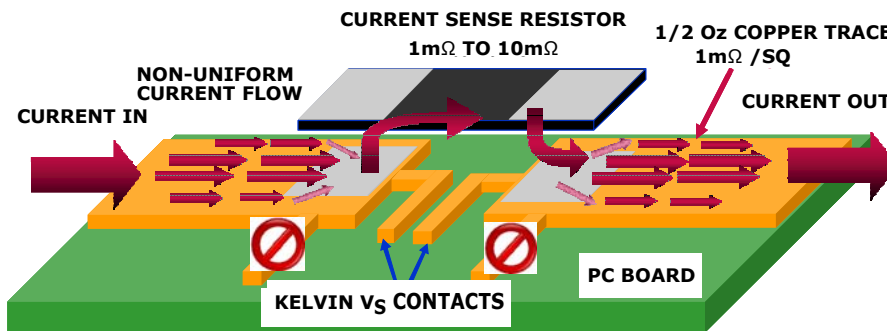


FIGURE 69. PC BOARD CURRENT SENSE KELVIN CONNECTION

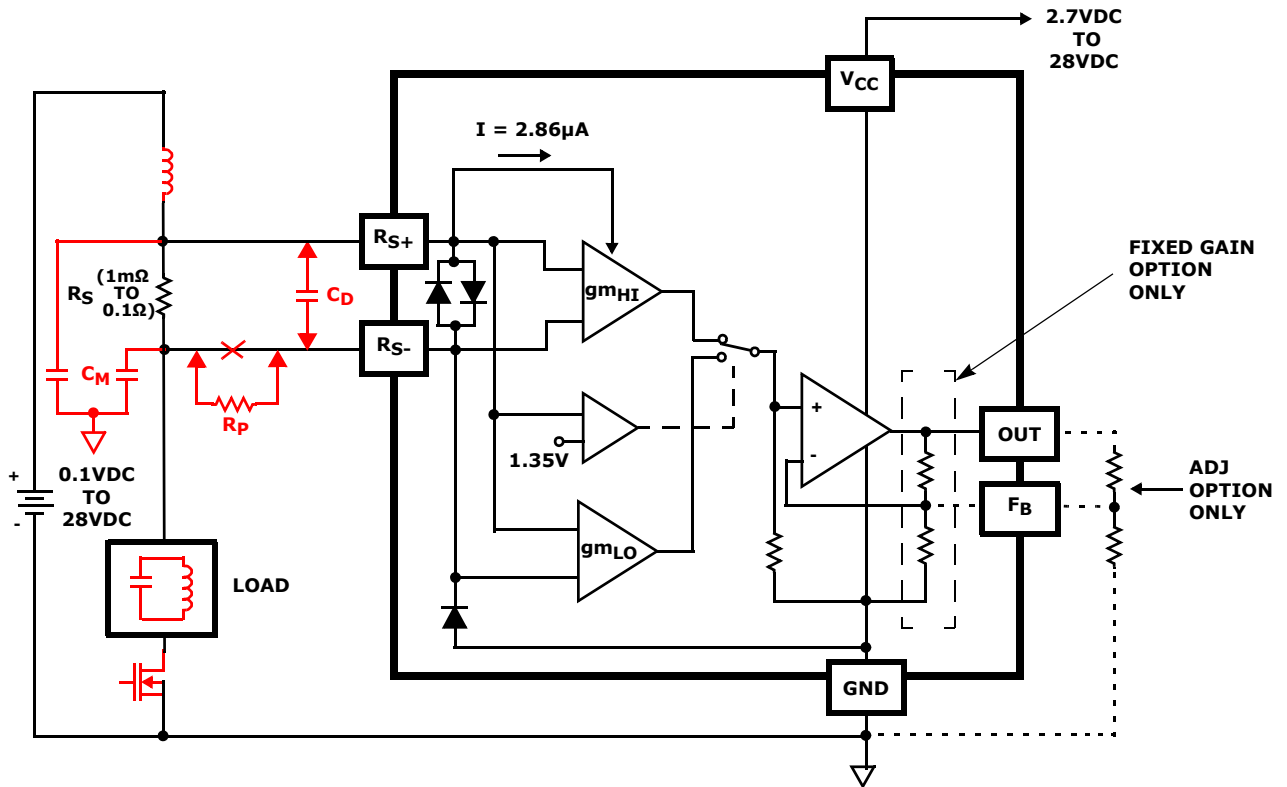


FIGURE 70. TYPICAL APPLICATION CIRCUIT

**Overall Accuracy (VOA %)**

VOA is defined as the total output accuracy Referred-to-Output (RTO). The output accuracy contains all offset and gain errors, at a single output voltage. Equation 4 is used to calculate the % total output accuracy.

$$V_{OA} = 100 \times \left( \frac{V_{OUT\text{actual}} - V_{OUT\text{expected}}}{V_{OUT\text{expected}}} \right) \quad \text{(EQ. 4)}$$

where

$$V_{OUT\text{Actual}} = V_{SENSE} \times \text{GAIN}$$

Example: Gain = 100, For 100mV VSENSE input we measure 10.1V. The overall accuracy (VOA) is 1% as shown in Equation 5.

$$V_{OA} = 100 \times \left( \frac{10.1 - 10}{10} \right) = 1\% \quad \text{(EQ. 5)}$$

**Power Dissipation**

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (TJMAX) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 6:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times P_{D\text{MAXTOTAL}} \quad \text{(EQ. 6)}$$

where:

- PD<sub>MAXTOTAL</sub> is the sum of the maximum power dissipation of each amplifier in the package (PD<sub>MAX</sub>)
- PD<sub>MAX</sub> for each amplifier can be calculated using Equation 7:

$$P_{D\text{MAX}} = V_S \times I_{q\text{MAX}} + (V_S - V_{OUT\text{MAX}}) \times \frac{V_{OUT\text{MAX}}}{R_L} \quad \text{(EQ. 7)}$$

where:

- T<sub>MAX</sub> = Maximum ambient temperature
- θ<sub>JA</sub> = Thermal resistance of the package
- PD<sub>MAX</sub> = Maximum power dissipation of 1 amplifier
- V<sub>CC</sub> = Total supply voltage
- I<sub>qMAX</sub> = Maximum quiescent supply current of 1 amplifier
- V<sub>OUTMAX</sub> = Maximum output voltage swing of the application

R<sub>L</sub> = Load resistance

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/12/10	FN6548.3	Added Note 4 to Part Marking Column in "Ordering Information" on page 3. Corrected hyperlinks in Notes 1 and 3 in "Ordering Information" on page 3.
4/8/10		Removed "Coming Soon" from evaluation boards in "Ordering Information" on page 3.
4/7/10		Added "Related Literature*(see page 23)" on page 1 Updated Package Drawing Number in the "Ordering Information" on page 3 for the 20V, 50V and 100V options from MDP0038 to P50.64A. Revised package outline drawing from MDP0038 to P5.064A on page 24. MDP0038 package contained 2 packages for both the 5 and 6 Ld SOT-23. MDP0038 was obsoleted and the packages were separated and made into 2 separate package outline drawings; P5.064A and P6.064A. Changes to the 5 Ld SOT-23 were to move dimensions from table onto drawing, add land pattern and add JEDEC reference number.
3/10/10	FN6548.2	Releasing adjustable gain option. Added adjustable block diagram (Page 2), Added adjustable gain limits to electrical spec table, added Figures 47 through 60, Added +85°C curves to Figures 6 thru 14, 20 thru 28, 34 thru 42, and Figures 48 thru 56. Modified Figure 70.
2/4/10	FN6548.1	-Page 1: Edited last sentence of paragraph 2. Moved order of GAIN listings from 20, 50, 100 to 100, 50, 20 in the 3rd paragraph. Under Features ....removed "Low Input Offset Voltage 250µV, max" Under Features .... moved order of parts listing from 20, 50, 100 (from top to bottom) to 100, 50, 20. -Page 3: Removed coming soon on ISL28006FH50Z and ISL28006FH20Z and changes the order or listing them to 100, 50, 20. -Page 5: VOA test. Under conditions column ...deleted 20mV to. It now reads ... Vsense = 100mV SR test. Under conditions column ..deleted what was there. It now reads ... Pulse on RS+pin, See Figure 51 -Page 6: ts test. Removed Gain = 100 and Gain = 100V/V in both description and conditions columns respectively. -Page 9: Added VRS+= 12V to Figures 16, 17, 18. -Page 11: Added VRS+= 12V to Figures 30, 31, 32. -Page 13 & 14: Added VRS+= 12V to Figures 44, 45, 46. -Page 14 Added Figure 51 and adjusted figure numbers to account for the added figure. -Figs 8, 26, and 40 change "HIGH SIDE" to "VRS = 12V", where RS is subscript. -Figs 9, 27, and 41 change "LOW SIDE" to "VRS = 0.1V", where RS is subscript.
12/14/09	FN6548.0	Initial Release

## Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to [www.intersil.com/products](http://www.intersil.com/products) for a complete list of Intersil product families.

\*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL28006](http://www.intersil.com/ISL28006)

To report errors or suggestions for this datasheet, please go to [www.intersil.com/askourstaff](http://www.intersil.com/askourstaff)

FITs are available from our website at <http://rel.intersil.com/reports/search.php>

---

For additional products, see [www.intersil.com/product\\_tree](http://www.intersil.com/product_tree)

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

---

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

---

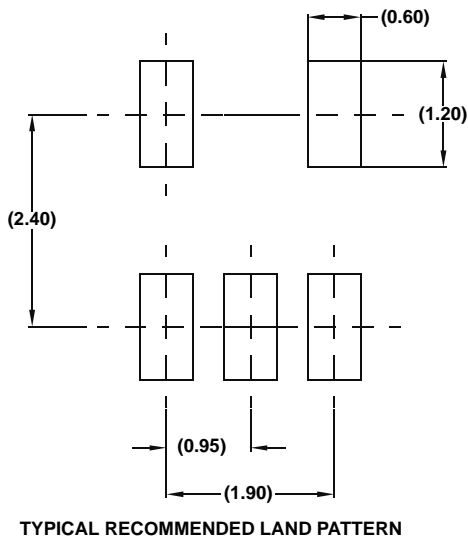
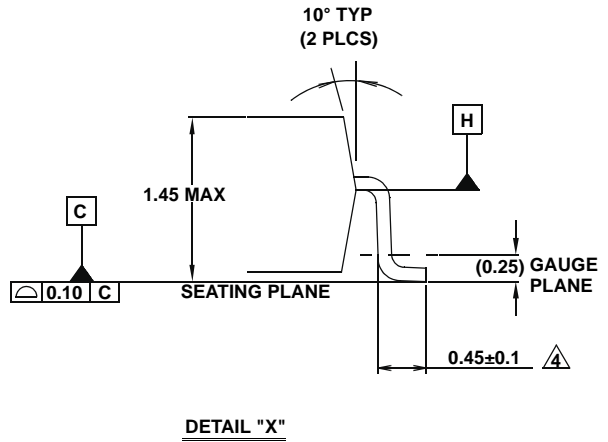
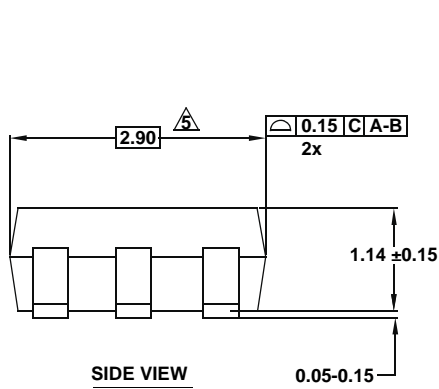
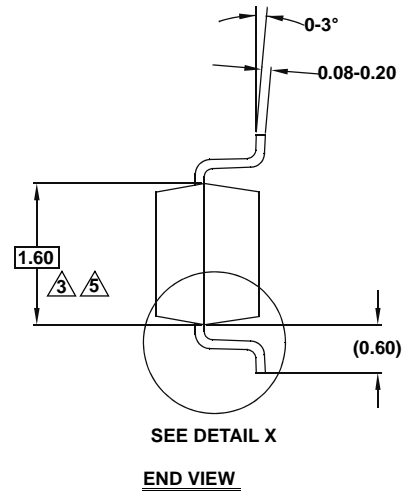
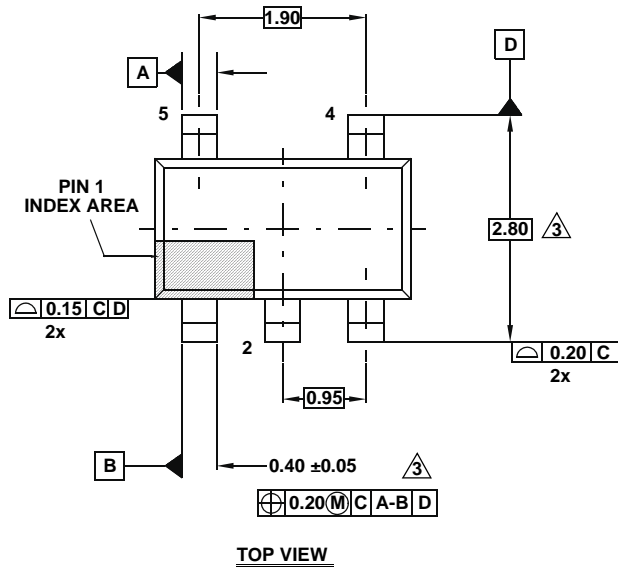
For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

# Package Outline Drawing

## P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 0, 2/10



**NOTES:**

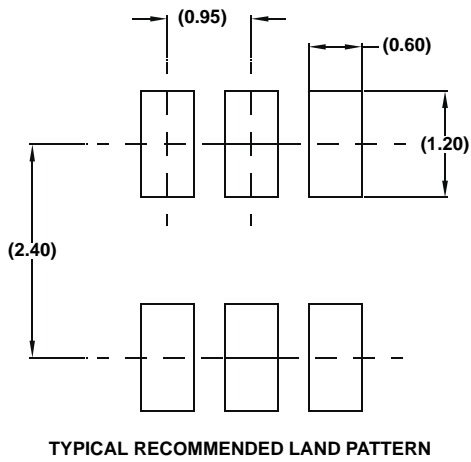
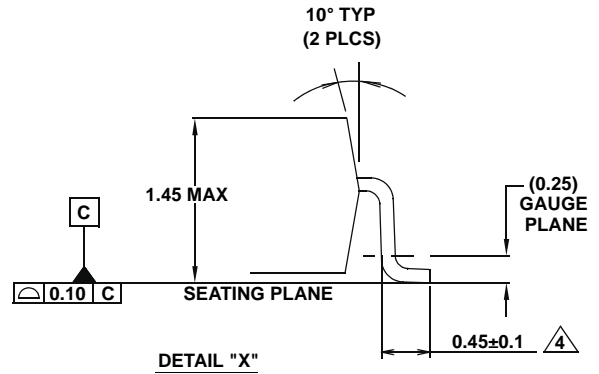
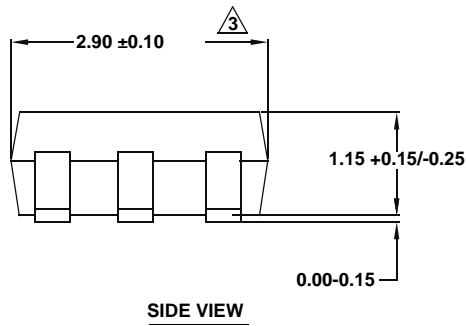
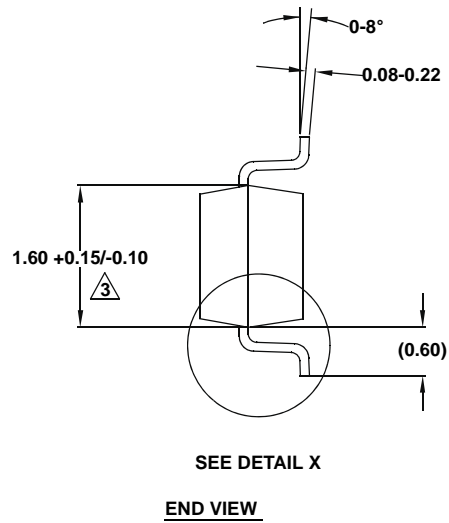
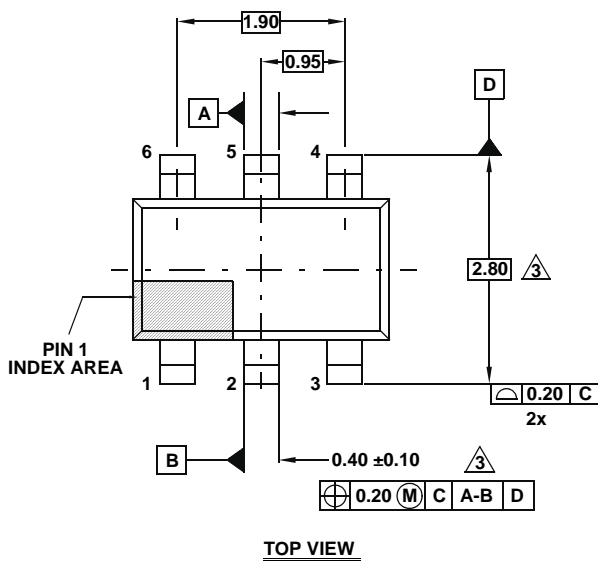
1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. This dimension is measured at Datum "H".
6. Package conforms to JEDEC MO-178AA.

# Package Outline Drawing

## P6.064

### 6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 4, 2/10



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. Package conforms to JEDEC MO-178AB.